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| 25 | 8/6/2020 | Version refreshed for the collabnet review |
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| 27 | 25/6/2020 | Modifications :  -add details about isolation constraint for IP owners with PPD(chap3.2)  -add details in power down/up of txbist and rxbist in 4.2.2 and 6.2.2  -change supply for bb bist to 0.9V and BD updated  -add trigstop signal for RXbist 5.2  -txbist\_enable description updated 6.2  -isolation txbist updated 6.8 |
| 28 | 29th June 20 | Correct power mode after review with marcello/francoise |
| 29 | 2nd of july | Update I/O of rxbist digital, add power controls diagram description from marcello |
| 30 | 3rd of july | Change settling time and vga gain for txbist I?O for txbist and rxbist |
| 31 | 15th of july | -modifications of I/O txbist and rxbist analog  -spec cm output for PPD and TXbist added  -change Rload for bbbist (tbf)  -remove ssb\_pwr control  -LPF controls + 2 LPFs added for txbist and PPD VGA  -BBBist IMD2 changed to 70dbc  -add requirement for PPD, if>6dBm and <9dBm PPDout>response at 6dBm |
| 32 | 18th of august | Add DEM AS from Paul W |
| 33 | 25th of august | AR:Add noise spec chapter for BB bist  Correct some typo/spec  Align figure numbers  Update the “to be updated” chapters |
| 34 | 26th of august | DD : update I/O RXbist |
| 35 | 26th of august | AR: Correct SNR spec for BB BIST |
| 36 | 27th of august | Update TXBist I/O + change block diagram to allow double connections to ATB or TXADC |
| 37 | 31th of august | AR:Update PPD and RF Bist electrical specifications |
| 38 | 1st of sept and 2nd of sept | DD:remove d\_pon\_ldo, change names of enables for txbist, update I/O txbist |
| 29 | 8/9 | DD:update rxbist IO |
| 30 | 9/9 | DD&Laure : update I/O txbist and test settling time |
|  |  |  |
| 31 | 10/09 | DD:rename I/o PPD.  Spec update following subIP RS review |
| 32 | 21/9 | DD:changed PPD chapter for integration |
| 33 | 22/9 | AR: correction of interface width (aligned with register map)  Typo correction on spec (Aligned with Sub-IP RS)  Highlate sections to be updated  Dac bus changed to <255:0> |
| 34 | 14/10 | Updat RF BIST lineup  LO doubler and SSB out power calibration algorithm |
| 35 | 09/11 | Remove LPF for tx and ppd  Clarification of powerdown current |
|  | 24/11 | Change spec for currnt consumption baseband |
| 36 | 14/01 | AR: general corrections, alignment with Rs/sub-IP Rs, add BB filter trim |

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# Content-README

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Make sure you are starting from the last version in collabnet

When modifying, as the document is in tracking mode > Go to review>accept all changes so that your modifications will be visible

Update revision history

# RFBIST overview

This document is the architectural description of the smartTRX Bist and is the technical answer to the requirement specification (RS) that can be found in DOORS :

<https://doorsng.nxp.com/rm/web#action=com.ibm.rdm.web.pages.showProjectDashboard&componentURI=https%3A%2F%2Fdoorsng.nxp.com%2Frm%2Frm-projects%2F_r8ZsYRVKEeiLn-6Dce4MoA%2Fcomponents%2F_UmtRABLKEeqkS9nHNrfCpg&oslc.configuration=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136>

This document is supported by a feasibility document demonstrating the feasibility of the architectures chosen :

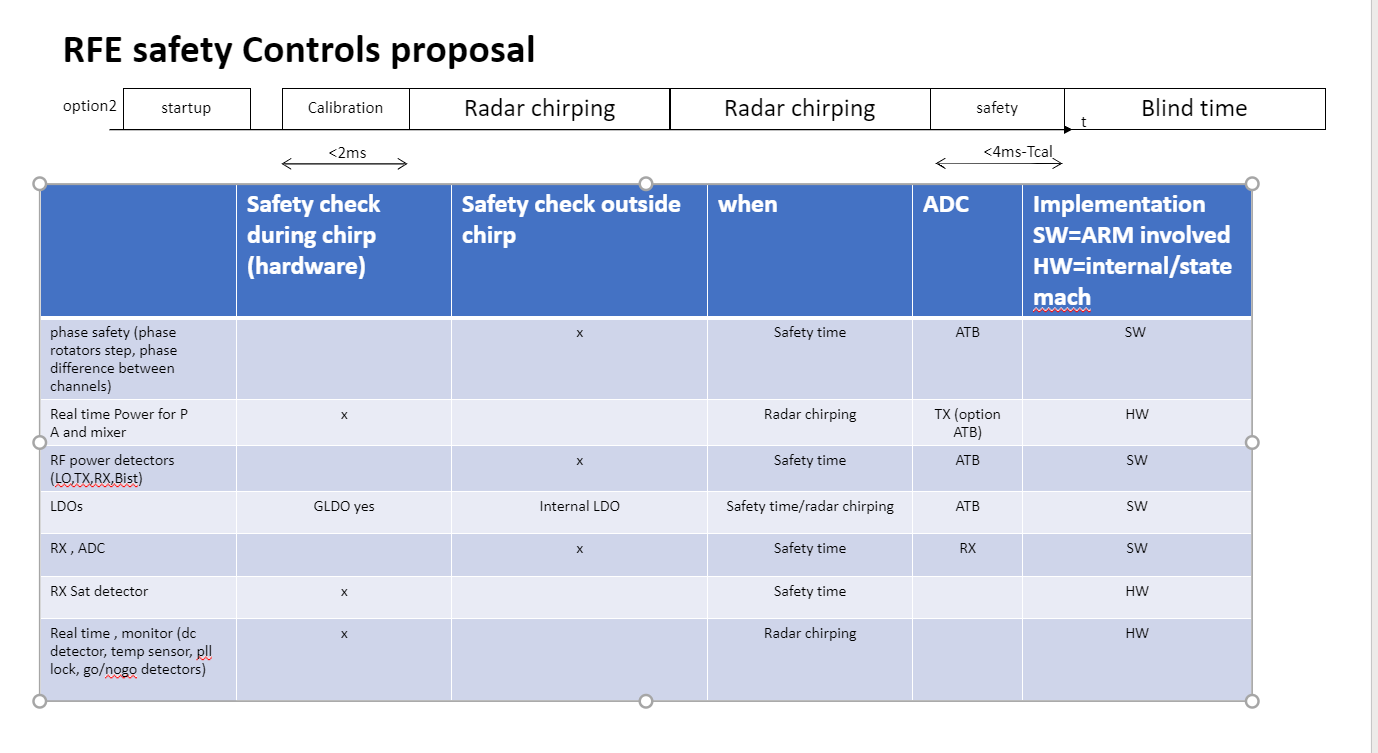
<https://www.collabnet.nxp.com/sf/go/doc418673?nav=1&pagenum=1&pagesize=15>

The status of the Architecture document is :

* Internally reviewed by the Bist team
* Feasibility not fully finished. Open questions are in RED (especially for the PPD)

The BIST means “Built in self test”. This corresponds to additional circuitry and process which allow to test the RFFE without the use of external instruments. This circuitry can be used for several goals :

* Safety : constant check (power detector) or at specific time during the radar sequence (safety time)
* Calibration : information from the bist can be used for calibration
* Test : used by the tester as a replacement of external RF instruments
* Lab : can be used in the lab to replace external equipments

Figure 1 Use of the BIST during operation

During operation BIST can be used at startup (for calibration and fault injection), before each chirp frame (for calibration) and after the frame (safety) There is no use of the Bist during chirping operations or between chirps [[art1098945](https://doorsng.nxp.com/rm/resources/_a443ba2c808e4930ae5f815a2b0a6984?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)][[artf1098974](https://doorsng.nxp.com/rm/resources/_6619653a3f7943dd917dfea510c8826d?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)]. Usually the chirp is controlled by the software through SPI.

The BIST is split into 3 categories which are described in 3 chapters :

* peak detector allows to measure the power level at different locations of the circuit
* RXBist : generate RF or baseband source to test the Receivers. It includes an analog and a digital control part
* TXBist : Measure TX phase difference. It consist on an analog part which after digital conversion is processed by the software

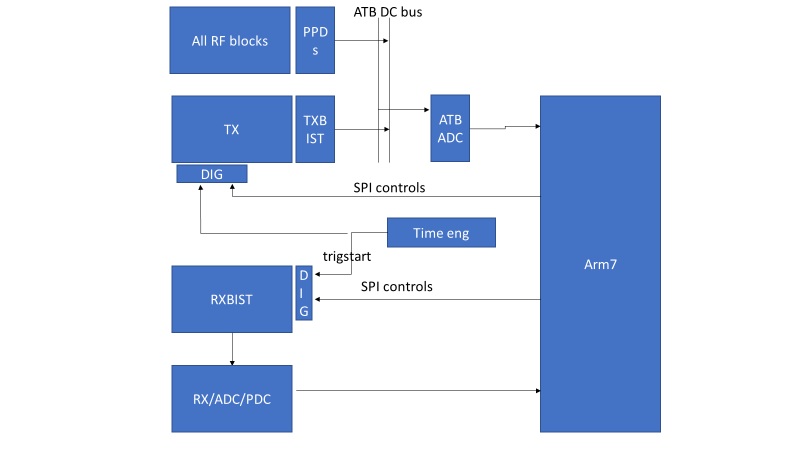


Figure 2: General block diagram overview

## Bist in Master / slave mode

The BIST is the slave of the software. The startup, powerdown are controlled by SPI. The phase synchronization between chips for the rX is managed through the trig\_start control signal

# peak detector (PPD)

## Description and Block diagram

Peak detector is based on voltage detection. It is then up to the integrator to make sure the power=>voltage conversion is correct (in the range of voltage as defined in the electrical specification, constant impedance to avoid error due to power=> voltage conversion).

The peak detector is accurate, has a high dynamic but is not linear and needs postprocessing conversion to get a voltage information independent of the temperature based on a temperature compensation conversion and a reference curve. The system is based on a 2 steps measurement (RF and without RF) to be insensitive of analog offsets. IT is up to the integrator to make sure the “off mode” is supported and gives sufficient attenuation.

Rms detector is not supported in smarttrx

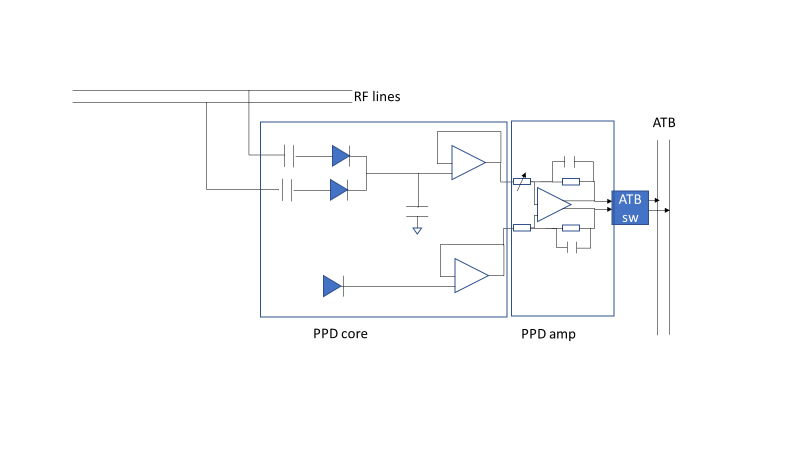
PPD is composed of a PPD core that can be measured directly by the ATB ADC (single ended ADC conversion). In some cases where the input level measured is too low a PPD amp with some voltage amplification must be added. In this case the ADC ATB is using the differential conversion modeGeneral Functionality and Operational mode

Figure 3: Coupler+PPD block diagram

Below is describes the list of PPD currently planned to be used in the RFE with its corresponding range and accuracy. The PPD analog informations are sent to the ATB ADC or TX ADC to optimize the measurement time (parallelization)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **blocks** | | **Input range (accuracy)** | **PPD amp** | | **ADC used** | | |
| SSB\_LOX2 | | 2.5dBm(+/-1) | VGA:0dB gain | | ATB ADC | | |
| SSB\_driver2 | | 4dBm(+/-1) | VGA:0dB gain | | ATB ADC | | |
| RX\_bist | | -10dBm(+/-0.35) | 10-20dB | | ATB ADC | | |
| RX\_Lomixer\*2 | | Handled by Rx team |  | | ATB ADC | | |
| TX\_PR | | -7dBm | VGA (SW ctrl for gain setting) | |  | | |
| TX\_LOx2 | | 2.5dBm(+/-1) | VGA 0dB gain cmmon with PR | | TX ADC | | |
| TX\_PAinput | | 5dBm(+/-1) | VGA 0dB gain cummon with PR | | TX ADC | | |
| Tx\_PA high+midle range | | 5dBm to 13,5dBm | 10-20dB | |  | | |
| TX\_PA low range | | <-10dBm(+/-0.35) | TBD | |  | | |
| LO\_RX(40G) | | [-6, 2](+/-1) | Used to get good CM for ADC | | ATB ADC | | |
| LO\_TX(40G) | | [-6, 2](+/-1) | Used to get good CM for ADC | | ATB ADC | | |
| LO\_out(40G) | | [0,6] (+/-1) | Used to get good CM for ADC | | ATB ADC | | |

Table 1: PPDs in RFE

The peak detector requires a double measurement (with and without signal). The peak detector measure firstly the reference Vout(no\_rf)-Vdummy(t0). The Vdummy allows to keep a reference at a certain time T0. It is considered that the we are able to turn off the RF signal in front of the PPD (idea is even to turn off the full RF buffers chain). This measurement can be done potentially at a time different than the power measurement (for example during the calibration time thanks to the dummy) but it is preferred to do the measurement sequentially The attenuation of the RF signal for the power off mode must be at least 25dB (tbf)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Level RF input | Accuracy expected | Error acceptedd due to offset | sensitivity | Equivalent input signal | isolation |
| 0dBm (225mv) | +/-1dB | +/-0.1dB (1%) | 20mv/dB=>max 2mv | 2mvout=>20mvpkin=>-20dBm | Min 21dB typ |
| -10 | +/-0.5dB | +/-0.05dB (1%) | 5mv/dB=>0.25mv | 0.25mv=>5mv | Min typ 23dB |

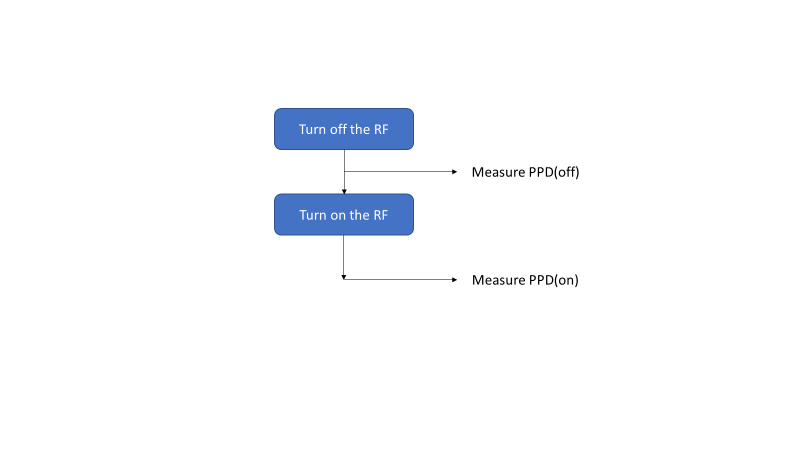


Figure 4: 2 steps measurement

Due to the unlinear response of the PPD, it requires a postprocessing (software) operation Voutpk(after postprocessing)=Vinpk=F(Vout(rf)-Vdummy(t1) – (Vout(no\_rf)-Vdummy(t0)). Notice F is a function of the temperature.

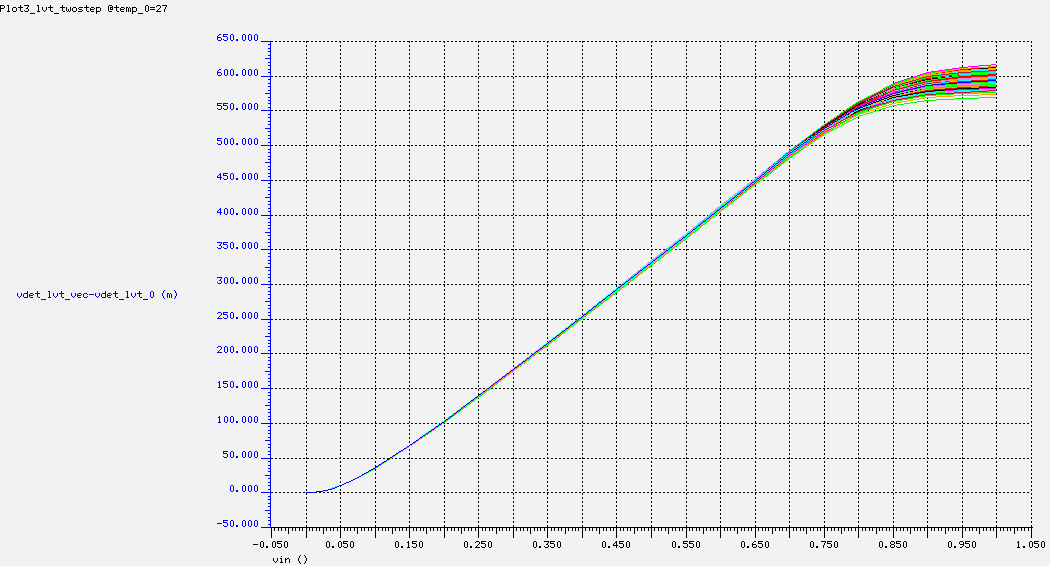


Figure 5: Output voltage of the PPD after 2 steps measurement

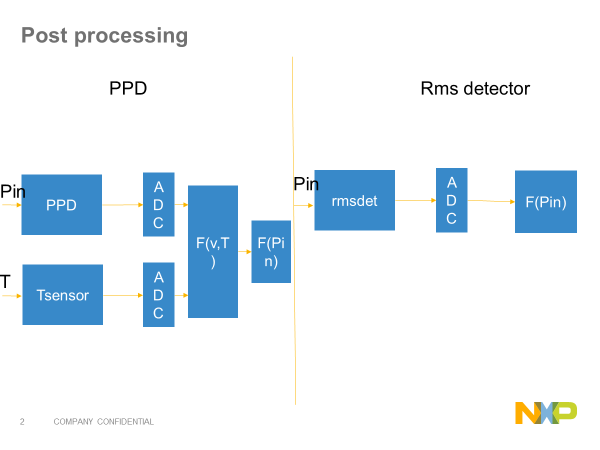


Figure 6: Overview of power detector processing

The reference function will be available during the design in the user guide.

Sources of errors for the PPD :

* Variation of the PPD analog
* Error due to the Gain variation (in VGA and in ADC). Error looks to be neglectable, no calibration planned
* Error due to reference curve (due to the temperature offset between temp sensor and PPD)
* Noise (attenuated by analog filtering and sliding averaing in the ATB block) => analog filtering removed snce contribution is neglectible
* ADC error (INL,DNL) can be small with VGA

A feasibility document express the errors contributors effect on the overall accuracy. This help to design the needed gain for each ppd to achieve the required accuracy.

Settling time of the signal to ATB input must be fast enough to be able to measure several peak detector in series while optimizing the total processing time. If needed, a sliding averaging in the ATB is required to reduce the noise impact (integrated in the ATB ADC digital).

### Calibration mode

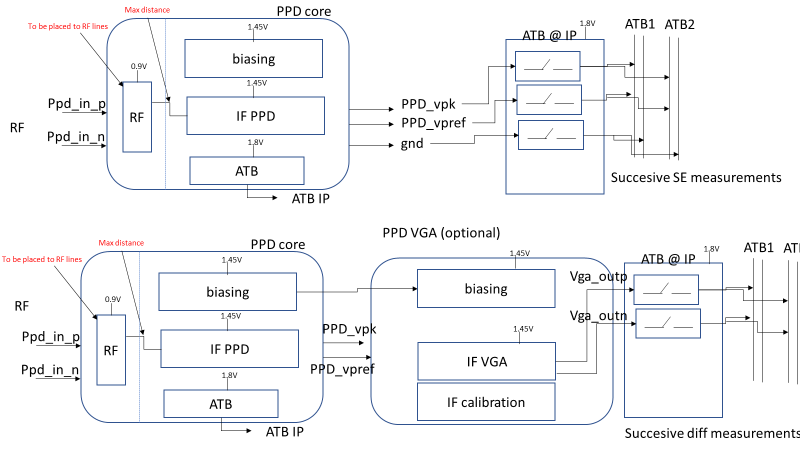
Given the high accuracy of the VGA, no calibration in needed (see feasibility document)

## Integration guide

### List of blocks

The final version will include 3 blocks : PPD core rf/if and VGA

At that time PPD core is called : BIST\_PPD\_top

VGA : BIST\_PPD\_vga

With a normal PPD connection the outputs are connected in single ended mode to the ATB ADC (common mode not supported). So it consists of 4 measurements Vpk.Vref w and wo RF.

When the VGA is put, the connection is differential and 2 measurements are needed, vpk-vref (wo rF) and vpk-vref (w RF)

### Integration constraints :

* Distance between RF lines and PPD should be short. IT is planned to put the RF part independent to place it close to the RF lines
* When PPD is used for monitoring power (and not voltage), it should be put placed such as the RF impedance load is not varying to insure a stable conversion PdBm to voltage.
* Distance between RF and IF lines (ppd\_core\_rf and ppd\_core\_if) should be < tbd um
* Supplies and ground strategy : RF supply/ground tbc to local supply/gnd of RF block to be measured
* Distance between ppd core and vga to discuss with franco
* Distance between ppd core and tb switches to discuss with franco

### Interface with external (PPD)

|  |  |  |  |
| --- | --- | --- | --- |
| pin | type | description | From/to |
| vdda\_ppd\_1v45 | supply | 1v45 supply for buffers and VGA | From local IP |
| vdda\_ppd\_0v9 | supply | Supply for PPD core | From local IP |
| vdda\_ppd\_1v8 | supply | Supply for ATB | From local IP |
| vssa\_ppd\_1v45 | ground | 1.45V ground | From local IP |
| vssa\_ppd\_0v9 | ground | 0.9V ground | From local IP |
| vssa\_ppd\_1v8 | ground | 1.8V ground | From local IP |
| ppd\_In\_p | RF | RF positive input | From local IP |
| ppd\_In\_n | RF | RF negative input | From local IP |
| ppd\_Vpk | DC-out | Pk voltage | To VGA/ADC |
| ppd\_vref | DC-out | Ref voltage | To VGA/ADC |
| d\_ppd\_en\_ls0v9 | Dig\_in | Enable ppd core | dig |
| d\_ppd\_buf\_en\_ls1v45 | Dig\_in | Enable buffer | dig |
|  |  |  |  |
| d\_ppd\_Atb\_ctrl\_ls1v8<3:0> | Dig\_in | Control atb output | dig |
| Ibias\_ppd\_20u\_bg\_in | DC-in | Bias current | to be provided locally |
| Ibias\_ppdtovga\_25u\_bg\_out | DC-out | Bias current | To vga |
| Atb\_p | DC-out | Atb positive outoput | To aTB1 or aTB2 |
| Atb\_n | DC-out | Atb negative outoput | To aTB1 or aTB2 |
|  |  |  |  |

Table 2: interface with external for the power detector

### Interface with external (VGA)

|  |  |  |  |
| --- | --- | --- | --- |
| pin | type | description | From/to |
| vdda\_ppd\_1v45 | supply | 1v45 supply for buffers and VGA | From local IP |
| vdda\_ppd\_1v8 | supply | Supply for ATB | From local IP |
| vssa\_ppd\_1v45 | ground | 1.45V ground | From local IP |
| vssa\_ppd\_1v8 | ground | 1.8V ground | From local IP |
| vga\_In\_p | DC-in | RF positive input | From local IP |
| vga\_In\_n | DC-in | RF negative input | From local IP |
| vga\_outp | DC-out | Pk voltage | To ADC |
| vga\_outn | DC-out | Ref voltage | To ADC |
| Ibias\_ppdtovga\_25u\_bg\_in | DC-in | 25uA current from PPD | From PPD\_core |
| d\_vga\_en\_ls1v45 | Dig\_in | Enable vga | dig |
| d\_vga\_atb\_ctrl\_ls1v8<3:0> | Dig\_in | Control atb output | dig |
| d\_vga\_gain\_ls1v45<2:0> | Dig\_in | Gain vga | dig |
| Atb\_p | DC-out | Atb positive outoput | To aTB1 or aTB2 |
| Atb\_n | DC-out | Atb negative outoput | To aTB1 or aTB2 |

Table 3: interface with external for the vga

### Supplies

1.45V (buffer/core) , 0.9V(ppd core diode), 1.8V(Atb).

Grounds : vssa\_ppd\_1v8,vssa\_ppd\_1v45\_vssa\_ppd\_0v9

### DFT

The diodes current and voltages should be measured in DC in test mode.

It should be possible to observe internal PPD and VGA nodes at: LDO voltage, copy of detector current ref, Bias voltages, Nbias and Pbias of amplifiers

## Electrical specifications

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | min | typ | max |  | Linked Doors RS | comment |
| Specification for the RF part | | | | | | |
| Supply for aTB switch | -7% | 1.8V | 7% |  |  | +/-5% full performance, +/-7% full fonctionality |
| Input LDO supply | 1.45V-7% | 1.45V | 1.45V+7% | V |  |
| Supply LDO out | 0.9V-7% |  |  | 0.9V+7% |  |
| RF range1 | 76 |  | 81GHz |  |  |  |
| RF range2 | 38 |  | 40.5GHz |  |  |  |
| RF range3 | 5GHz-tbd |  | 81GHz |  |  | For ATB |
| Input voltage range 1 | 110 |  | 1100 | mVpkd |  | Above 1100mVpkd voltage > voltage (1100mv) |
| Input voltage range 2 | 80 |  | 110 | mVpkd |  |  |
| Total input voltage range | 80 |  | 1100 | mVpkd |  | For PA cal |
| Accuracy of PPD core for input voltages range1 | -0.35 |  | 0.35 | dB |  | PVT&mismatch  accuracy of PPD in standalone (not including VGA, ADC) |
| Total PPD accuracy (including ADC) for input voltage range1 with ADC | -0.5 |  | 0.5 | dB |  |  |
| Sensitivity for input voltage range 1 |  | 10 |  | mv/dB |  | Sensitivity with VGA |
| Accuracy of PPD core for input voltage range 2 | -1 |  | 1 | dB |  |  |
| PPD core Vout | -0.1 |  | 0.7 | Vpkdiff |  |  |
| PPD core output common mode voltage | 0.25 |  | 1.1 | Vpkdiff |  |  |
| VGA input Vin\_N |  | 200 |  | mV |  |  |
| VGA input Vin\_P | 200 |  | 700 | mV |  |  |
| VGA gain range | 0 |  | 20 | dB |  |  |
| VGA gain step |  | 10 |  | dB |  |  |
| VGA gain accuracy | -0.1 |  | 0.1 | dB |  | TBC |
| VGA output noise |  |  | TBD | dBv/sqrt(Hz) |  |  |
| Settling time at ADC input(from no rF signal to RF signal) |  |  | 500 | ns |  | Incl parasitic line to aTB |
| VGA Output common mode voltage | 0.38 |  | 0.6 | V |  | Adc common mode |
| Input capacitance |  | 5 | 10 | fF |  |  |
| Startup time |  |  | 1 | us |  |  |
| Powerdown time |  |  | 1 | us |  |  |
| Output load for buffer | 2-tbf |  |  | Kohm |  | Depends on line and distance to ATB and RX buffer input impedance |
| Current consumption on 1.45V |  |  | 5 | mA |  | buffers |
| Current consumption on 0.9V |  |  | 100 | uA |  | Mainly VGA |

Table 3: Electrical specification power detector

## Design Decisions (logged in DOORS AS)

|  |
| --- |
| Power detector |
| Power detector is based on voltage peak detection. Impdeance of the measured voltage must be controlled to not have error on the power to voltage conversion |
| Power detector is based on a 2 steps measurement (with RF power, without RF power). The measurement is done in serie by controlling the previous RF buffer in a fast way |
| The PPD is able to measure all the power of the chip from 1GHz to 81GHz downto -15dBm (100Ohms) |
| A programmable amplification is added behind the PPD core to amplify the DC signal to be measured. |
| The power detector analog information is postprocessed in software to compensate for temperature and response non linearity vs input |
| PPDanalog information is sampled by the ATB ADC at 5MHZ and need a postprocessing sliding average from 2 to 16 samples in the ATB |
| PPD is using 0.9V, 1.45V |

# RXBIST Analog

## Block diagram

The RX Bist is composed of a SSB modulator and baseband high SFDR signals to generate RF signal at input of the RX and baseband signals at the input of the baseband. This choice has been made to simplify the design of the RF SSB by shifting the BB linearity measurement into the IF domain

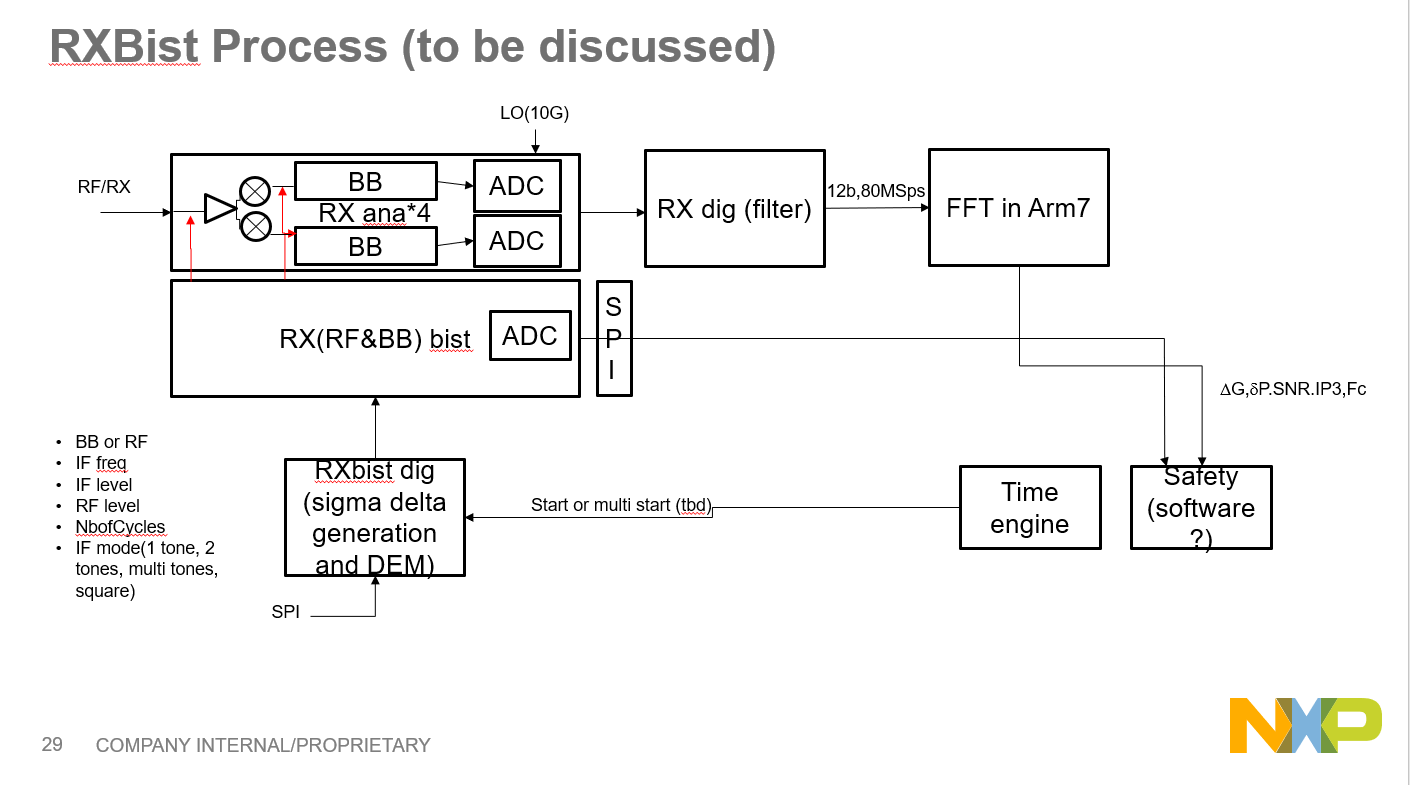


Figure 8: Overall block diagram Bist with digital

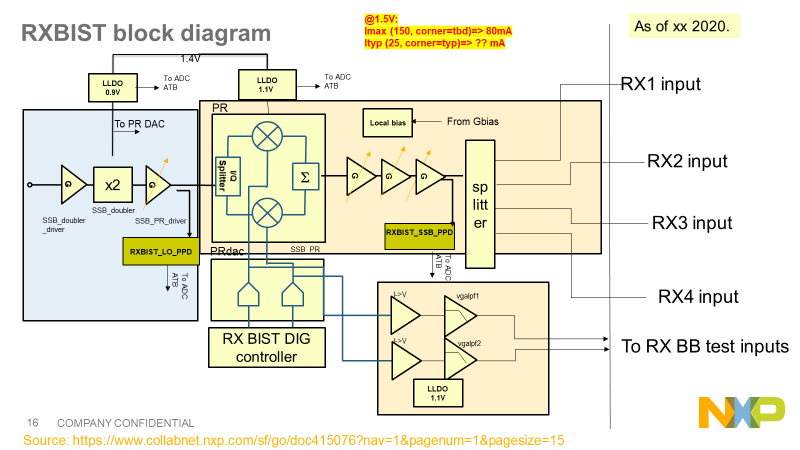


Figure 9: RX analog Bist block diagram

## General Functionality and Operational mode

### General functionality

The RXRF Bist is able to provide a programmable RF SSB signal simultaneously to the 4 receivers (see Figure 4) through a RF splitter. The RF signal is built from an IQ mixer that is mixing the LO signal with an IF signal. This signal is constructed from a digital signal converted with 2 DAC-8b to generate the IQ and hence the SSB signal.

The IF signal type is programmable. As the receiver is an IQ receiver the SSB doesn’t need high image rejection

The RXbist is interfacing with the LO doubler built with a 40GHz buffer, a frequency doubler to generate the 80GHz and a buffer to drive the phase rotator. The design is managed in the LO interface work package and the matching network will be optimized in the bist to guarantee a min power of 2.5dBm

The RF power is calibrated at the SSB output to guarantee a minimum power at the RX bist inputs (-10dBm). The power at the rX inputs are measured through precise power detector to guarantee the RX gain measurement accuracy[[art1098952[](https://doorsng.nxp.com/rm/resources/_77286326f50e4783b67cd6f733cf7d90?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) Also it is assumed (and have to be taken into account in the RX) that the phase and the gain linked to the coupler is not influenced by the impedance seen on RX (S11>7dB)

Dac Bias current should be able to calibrate SSB mod max power to it's nominal value over PVT

Buffers bias current tuning should be able to achive output power dynamic range (from max to min power)

The RX Bist can be set in 2 modes with the bistrx\_mode bit (0=RFbist, 1=BBBist).

### Power modes

From the outside there are 4 main digital signals that control the IP functional states. These states are described in Table 4.

|  |  |  |
| --- | --- | --- |
| State | Note | Controls |
| Off | The lowest power state. Everything is off. The pon\_ls\_rxbist is forcing all signals to analog block to 0. | pon\_ldo\_rxbist=x  pon\_ls\_rxbist=0  en\_rxbist=x  fast\_enable\_rxbist=X |
| #### | Ldo “enable” are activated but LDO are off | pon\_ldo\_rxbist=0  pon\_ls\_rxbist=1  en\_rxbist=x  fast\_enable\_rxbist=X |
| Standby | LDO are turned on | pon\_ldo\_rxbist=1  pon\_ls\_rxbist=1  en\_rxbist=x  fast\_enable\_rxbist=X |
| Fast turn on | Transition state between the standby and on states. The fast\_enable is high, which shorts the R in the bias RC filters to quickly charge the filter C and allow for fast settling. This state will last 1us. | pon\_ldo\_rxbist=1  pon\_ls\_rxbist=1  en\_rxbist=1  fast\_enable\_rxbist=1 |
| On | The IP is fully active and can be used bist | pon\_ldo\_rxbist=1  pon\_ls\_rxbist=1  en\_rxbist=1  fast\_enable\_rxbist=0 |

Table 4 RXbist functional power-states

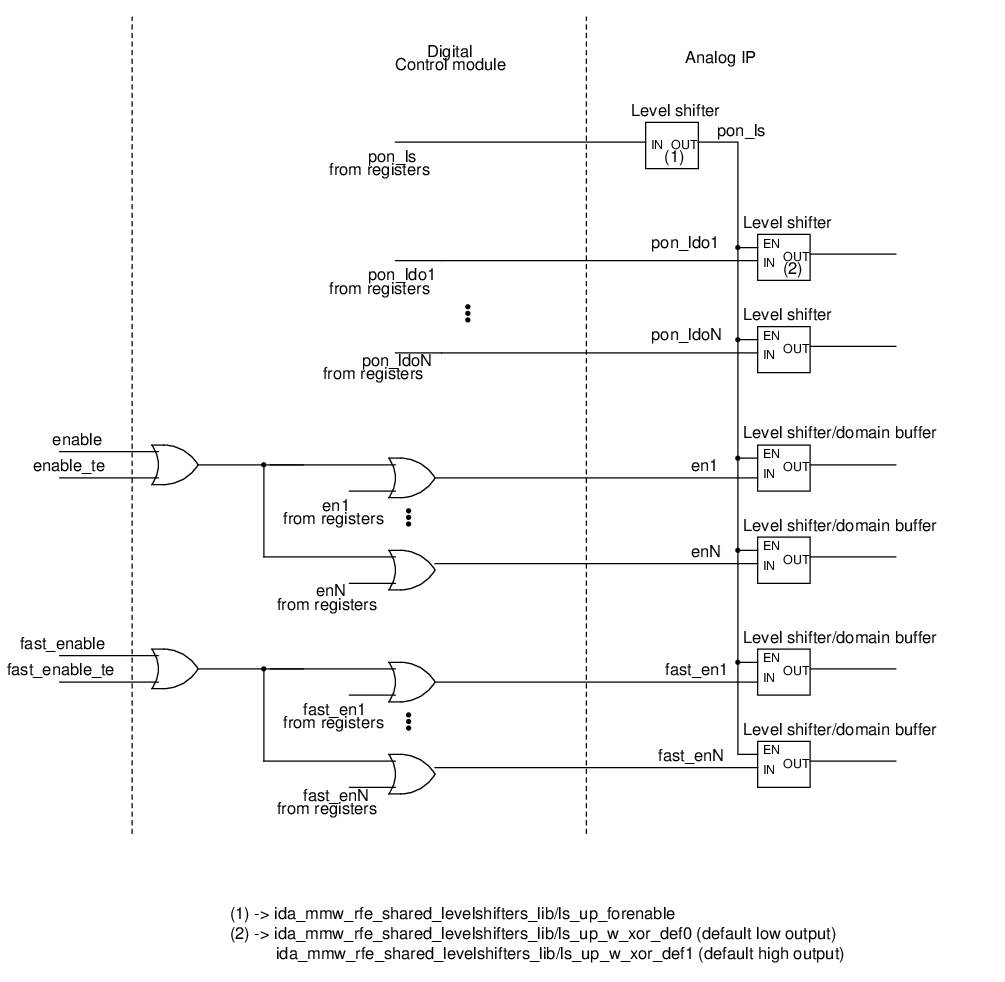


Figure 10: control of the Bist IP (to be updated)

## Interface with external

### I/O analog RXbist

*N.B: Updated interface can be found in the register map in this* [*link*](https://www.collabnet.nxp.com/sf/docman/do/viewDocument/projects.smarttrx/docman.root.es0.011_ic_architecture_design_and_i.non_fdo_documents.rfe.ip_rtl_dev_automation.reg_map_xls_for_all_ips/doc433591)

|  |  |  |  |
| --- | --- | --- | --- |
| pin | type | description | From/to |
| d\_dac\_i<255.:0> | Dig/in | Digital control I | RXbist dig |
| d\_dac\_q<255:0> | Dig/in | Digital control q | RXbist dig |
| LOin | RF /in | 38GHz input | LO |
| SSBout<3:0> | RF/out | 77GHz RF signal | RX |
| BBoutIn/p | Ana/out | IF signal I | To:RX |
| BBoutQn/p | Ana/out | IF signal Q | To:RX |
| d\_bbbist\_cm\_sel<2:0> | Dig/in | common mode sel |  |
| d\_bbbist\_gain | Dig/in | Control of BBbist buffer gain(d\_bbbist\_gain) | OCII |
| d\_bbbist\_att <5:0> | Dig/in | Control attenuation at BBbist out | OCII |
| d\_bbbist\_rauchfilter\_cal\_tun<2:0> |  | Control filter tune caps |  |
| d\_ssb\_gain\_buffer1<5:0> | Dig/in | control of the gain buffer1 SSB | OCII |
| d\_ssb\_gain\_buffer2<5:0> | Dig/in | control of the gain buffer2 SSB | OCII |
| dac\_trim\_bias<4:0> | Dig/in | PR DAC trimming | OCII |
| D\_atb1\_en | Dig/in | Enable atb1 | OCII |
| D\_atb2\_en | Dig/in | Enable atb2 | OCII |
| d\_atb1<59:0> | Dig/in | ATB switches control | OCII |
| d\_atb2<59:0> | Dig/in | ATB switches control | OCII |
| d\_lox2\_ctrl<3:0> | Dig/in | Control of the LO\_bias current | OCII |
| d\_rxbist\_mode | Dig/in | Control DAC out switches to choose BBBist or RFbist | OCII |
| d\_psdac\_en  d\_ssb\_bias\_en  d\_dac\_buf1\_en  d\_dac\_buf2\_en  d\_lox2\_en  d\_lox2\_bias\_en  d\_bbbist\_cm\_en  d\_bbbist\_follo\_en  d\_bbbist\_lvls\_en  d\_bbbist\_rauch\_en  d\_psdac\_bias\_en  d\_pr\_en  d\_ppd\_ssb\_buf\_en  d\_ppd\_ssb\_buf\_en  d\_ppd\_lox2\_buf\_en  d\_ppd\_lox2\_en | Dig\_in | enable the IP (current is flowing) after its LLDO is enabled (0.9V supply is assumed present)  Enablig of :  -DAC (d\_psdac\_en)  -buffers(d\_ssb\_en)  -LO doubler(d\_lox2\_en)  -baseband(d\_bbbist\_en).  -PPD SSB (d\_ssbppd\_en) and PPD LO D\_lo\_ppd\_en  -PR (d\_prbist\_en) | dig |
| d\_rxbist\_fast\_en | Dig\_in | enable signal that stays high only for some time to short the R inside IP RC circuit (of a mirror for example(low noise mode if needed) | dig |
| Ibias\_rxbist\_flat | in | 90uA bg current from Gbias(2% trimmed) | From Gbias |
| Ibias\_rxbist\_ptat | in | 90uA ptat current from Gbias(2% trimmed) 0.213uA/K(see [[1]](#footnote-1)  ) | From Gbias |
| Ibias\_ldo\_rxbist\_0v9 | in | 20u Bias current for LDO 0.9V | From Gbias |
| Ibias\_ldo\_rxbist\_1v1 | in | 20u Bias current for LDO 1.1V | From Gbias |
| Ibias2\_ldo\_rxbist\_1v1 | in | 20u Bias current for 2nd LDO 1.1V | From Gbias |
| d\_xor\_feedback\_out<3:0> | digout | Xor scan chain feedback chain1 | dig |
| d\_xor\_feedback\_idac\_out<4:0> | digout | Xor scan chain feedback chain2 | dig |
| d\_xor\_ feedback\_qdac\_out<4:0> | digout | Xor scan chain feedback chain3 | dig |
| d\_xor\_ feedback\_atb1\_out<1:0> | digout | Xor scan chain feedback chain4 | dig |
| d\_xor\_ feedback\_atb2\_out<1:0> |  |  |  |
| d\_hvst\_en | digin | Activate hvst mode | OCII |
| d\_ldo\_lo\_en | digin | Activate LDO1 | OCII |
| d\_ ldo \_rf\_en | digin | Activate LDO2 | OCII |
| d\_ ldo \_dig\_en | digin | Activate LDO4 | OCII |
| d\_ ldo \_lo\_bp | digin | Bp mode LDO1 | OCII |
| d\_ ldo \_rf\_bp | digin | Bp mode LDO2 | OCII |
| d\_ ldo \_dig\_bp | digin | Bp mode LDO4 | OCII |
| d\_ ldo \_lo\_bypass | digin | Activate bypass mode LDO1 | OCII |
| d\_ ldo \_rf\_bypass | digin | Activate bypass mode LDO2 | OCII |
| d\_ ldo \_dig\_bypass | digin | Activate bypass mode LDO4 | OCII |
| d\_ ldo \_lo\_capvstress<1:0> | digin | LDO1 vstress cap | OCII |
| d\_ ldo \_rf\_ capvstress<1:0> | digin | LDO2 vstress cap | OCII |
| d\_ ldo \_dig\_ capvstress<1:0> | digin | LDO4 vstress cap | OCII |
| d\_pon\_ctrl\_pon\_ls | digin | Enable Lesvel shifter | OCII |
| d\_pr\_trim\_iso\_load<1:0> |  | Trimming of LO | OCII |
| D\_pr\_trim\_bias<1:0> | digin | PR bias trimming | OCII |
| d\_dft\_ctrl\_dac\_buf1\_range1 | Dig/in | Struct test for buf2A dac | OCII |
| d\_dft\_ctrl\_dac\_buf1\_range2 | Dig/in | Struct test for buf2A dac | OCII |
| d\_dft\_ctrl\_dac\_buf2\_range1 | Dig/in | Struct test for buf2B/2C dac | OCII |
| d\_dft\_ctrl\_dac\_buf2\_range2 | Dig/in | Struct test for buf2B/2C dac | OCII |
| d\_dft\_ctrl\_prdac\_en | Dig/in | Struct test for prDac | OCII |
| D\_dft\_ctrl\_biasdac\_en | Dig/in | Struct test for Dac | OCII |
| Rxbist\_spare<19:0> | digin | Spare bits | OCII |
| Rxbist\_spare\_in<3:0> | digout | Spare signals into digital |  |

Table 5: I/O RXBIST

### Usage with the RX

The RF signal can be fed directly at LNA input or LNA output. [[artf1098948](https://doorsng.nxp.com/rm/resources/_1e80c46f1eb842d58bab67b1ae1cbf21?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)] [[artf1098953](https://doorsng.nxp.com/rm/resources/_1e80c46f1eb842d58bab67b1ae1cbf21?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)][[artf1098946](https://doorsng.nxp.com/rm/resources/_8439cd8ea0764e4bbfd7f824c8f7c31d?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)] These controls are managed inside the RX modules.

The baseband signal generation allow to generate IF signal covering the RX bandwidth with a high linearity. The I and Q signal are buffered and sent to each of the RX baseband inputs. As the distance between RXbist and RX is high, the signals must be locally buffered to keep the signal bandwdith while driving the high capacitive load of the vgas. Different access is planned to be able to drive signal or monitor signals inside the baseband. [artf1098948][[[art1204765](https://doorsng.nxp.com/rm/resources/MB_183082ea7cd64c80a014f9524aa21a82?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)]

The Bist generation is used with the FFT embedded processing (FFT) and software [[artf1098944](https://doorsng.nxp.com/rm/resources/_0a797286ca6c4060806fd0cda2ba6de8?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)] that analyses the received signal : level, phase, harmonics.

Rx interface (I path) with Bist; ADC and ATB I/O. Each line is differential.

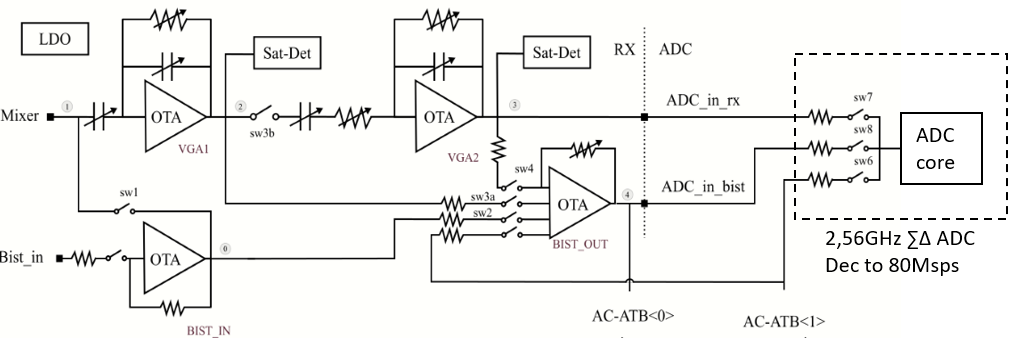


Figure 11: baseband test access

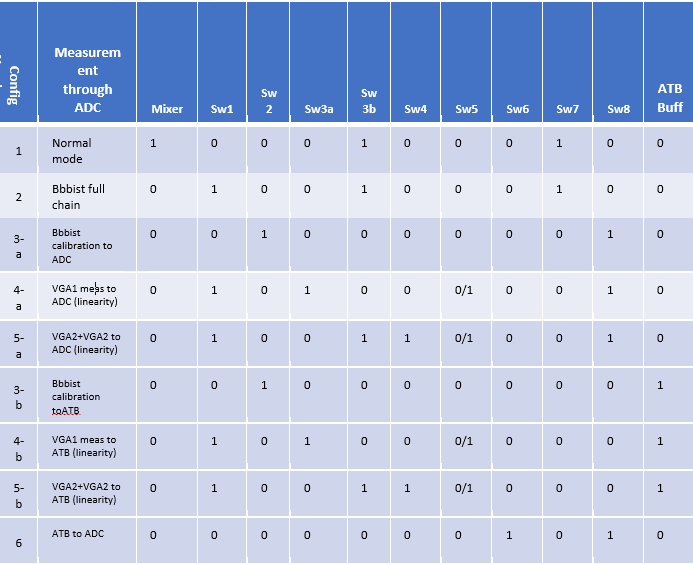


Table 6: Baseband Bist modes of operation

## Description of the block

The block is composed of :

* LO doubler chain (to multiply by 2 the input LO) with power detector control
* an IQ mixer (from TX) without calibration for minimum image rejection
* programmable buffers and splitter to get a 4dBm out with power detector having high accuracy
* 2 DAC 8b (from TX) (Thermometric DAC with <0:255>
* 3 LDO with supply monitors
* An OCII

The block is similar to the TX channel except :

* The DAC output is switchable from RF mode to BB mode
* the PA is replaced by a splitter by 4, the output power must be >4dBm to get good measurement with power detector at the rx side.
* The RF output power must be programmable with some dynamic. It is controlled by the DAC of the IQ modulator and buffers current controlled

### RF Lineup:

The SSB modulator must generate a signal that can be measured with the power detector at the receiver input with enough accuracy .

* With this power the RX chain should not saturate to be able to measure a reference level at ADC out. This reference is used to calibrate the full RX chain gain.
* When the reference is known, the level at SSB output power can be modified with the driver currents and Phase modulator.
* A reference level of >4dBm is calibrated through the SSB\_ppd detector (see calibration chapter)
* the step is controllable to allow measurement of vga while keeping same power at output
* SSB modulator must generate a signal into RF input that can be measured through ADC. Thus level at the ADC must be below ADC clipping which is Vclip=0.6Vp.

In the RF path, PPD is used to calibrate all power measurements. Thus, ppd must be the closest possible to the Rx chain to have maximum accuracy between ppd and LNA input.

PPD has good accuracy around -10dBm. It is placed after the splitter where the output power is around this value as shown in the table below:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | RF BIST out | Splitter Loss | Line+2nd splitter loss | Coupler directivity + matching losses | RF BIST to ADC in |
| Gain [dB] |  | -14 | -5 | -18 |  |
| Power Out [dBm] | 4 | -10 | -15 | -33 | -25 dBv |

Table 8: Power line-up at different stages of RFBist

With RFbist out of 4dBm, the power at the input of the ADC is:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| AGC | CGv (From ARP to ADC in) | | | Bist level at ADC in [dBv] | | |
|  | Min | Typ | Max | Min | Typ | Max |
| 0 | 23 | 25 | 27 | -28 | -26 | -24 |
| 1 | 26 | 28 | 30 | -25 | -23 | -21 |
| 2 | 29 | 31 | 33 | -22 | -20 | -18 |
| 3 | 32 | 34 | 36 | -19 | -17 | -15 |
| 4 | 35 | 37 | 39 | -16 | -14 | -12 |
| 5 | 38 | 40 | 42 | -13 | -11 | -9 |
| 6 | 41 | 43 | 45 | -10 | -8 | -6 |
| 7 | 44 | 46 | 48 | -7 | -5 | -3 |

Table 7: Max input RFBist power before saturating ADC

ADC clips for Vin>-7dBv. That allows power measurements for AGC 0 to 5 given to the above. For other AGC, the RFbist power is decreased through the buffer controls and PR DAC . All the measurement must be then relative to the initial measurement (SSB power maximum measured after the ADC) to keep the accuracy.

To be able to check the full AGC we need at least 7dB of dynamic (target 20dB)

The steps and dynamic are built from the buffers/PR current controls. Fine tuning can be done with digital cos/sin control.

### BB Lineup:

The DDS should provide a signal to measure the full range of the ADC by using the VGA

* The DDS should provide a signal that doesn’t saturate the VGA’s with the maximum gain
* The DDS should generate signals to test the saturation detectors of vga1 and vga2
* the step is controllable to allow measurement of sat detectors (vgas,ADC)
* BB signals allow to measure gains and linearity. For this purpose the BB buffer should provide a signal that saturate VGA1, but also a signal in the linear zone for max gain. These two conditions determines the range of the baseband bist signal power at the input of each Rx.
* VGA saturates around -6dBv. With maximum gain for VGA1 of 20dB. The Bist input level must be around -6-20+3=-23dBv (3dB of margin).
* On the other hand, for Rx-IF max gain (40dB) the output should be below ADC clipping level of -7.5dBv (0.6Vdp). Also IMD measurement must be done at least 10dB below Saturation of VGA2=-6dBv. This gives a lower requirement for BB-bist of -56dBv.
* All ADC measurements in full scale will be done through Rx analog with IF limitations of Rx (linearity/noise)
* Steps can be fine tuned by the DDS and also by the attenuator/amplification (see Figure 8)

### BB Linearity constraint

* ADC SFDR spec are 70dBc (for signal >-30dBFs=-37dBv). With the range fixed before we can measure SFDR at -37dBv.
* However ADC SFDR at full scale cannot be done through Rx VGA amplification since this later creates harmonics above 70dBc
* To measure SFDR at full scale, BB-bist upper range must be extended to -5dBv with SFDR requirement s>70dBc. This seems to us hard requirement to achieve. Buffer linearity at this high voltage will limit the SFDR as for Rx VGAs so the target of SFDR is guaranteed only up to -20dBv out
* The system can generate a 2 tones to check the Continental and RX-RS linearity requirement which are:
* IIP2>44-CG (CG=40dB max) , 5fhp<f1,f2<flp f1,f2=-56dBm RF =>OIP2=34dBVp
* IIP3>14-CG (CG=40dB max) , 5fhp<f1,f2<flp f1,f2=-56dBm RF =>OIP3=4dBVp
* 3 tones . Considering F1 for baseband is not a contributor because it is low frequency and filtered. Notice that F1 can create IMD due to mixer but it is not supported in the bist

|  |  |  |
| --- | --- | --- |
| F2(80KHz,2.6MHz), | F3 | Spurs (relative to F1,F2) |
| 0.4fhp-36dBm RF | 0.5fhp(100KHz,3.2MHz),, -36dBm RF | >40dBc |
| 0.4fhp(80KHz,2.6MHz), -46dBm RF | 0.5fhp(100KHz,3.2MHz),, -46dBm RF | >50dBc |
| 4fhp(800KHz,25MHz) -66dBm RF (-76dBVp vga1 input) | 4.4fhp(880KHz,28MHz), -66dBm RF | >55dBc |
| 4fhp(800KHz,25MHz), -70dBm RF (-80dBVp vga1 input) | 4.4fhp(880KHz,28MHz),, -70dBm RF | >60dBc |

Consequence on switches linearity (in the RX) :

Spec for sw4, sw5, sw6:            OIP3 >23.5 dBVp;   OIP2>53.5 dBVp

Spec for sw3a:                              OIP3 >3.5 dBVp;   OIP2>33.5 dBVp

Spec for sw2: OIP3 > 9dBVp; OIP2> 44dBvp

Spec for sw1 and BB source:    OIP3 >-16.5 dBVp;   OIP2>13.5 dBVp

### BB Noise constraint

Rx SNR measurement is done with an On/Of measurement (see chapter 8.2). Thus, there is no direct requirement on baseband noise generation.

However, all Rx and ADC linearity measurements needs to be able to measure low level of IMDs with a limited time duration of the signal. This means that at ADC level the noise with a limited number of samples must be below the linearity to measure.

ADC SFDR measurement: noise spec

In order to measure simultaneously 4 Rx and do their fft, maximum number of sample possible is 512 per Rx channel. In the other hand, the hardest linearity measurement possible with the BIST is ADC linearity measurement. This measurement uses 1 tone at -20dBv and H3 must be observed at levels as low as -96dBv as shown by the figure below.

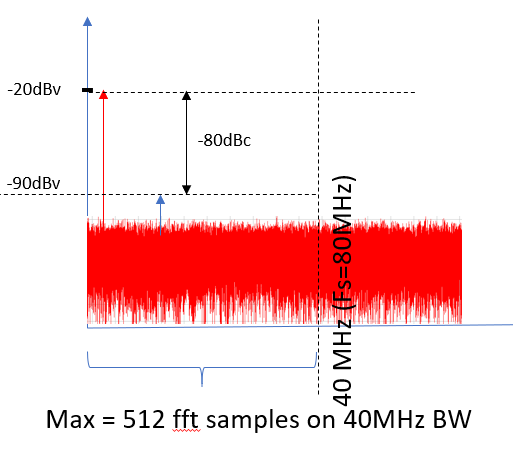


Figure 12: Noise consideration to observe linearity measurement

Having noise at least 10dB below H3 spec gives:

/

This noise level requirement is hard to obtain but possible. And it includes 10dB margin from linearity spec. This margin can be decreased if the requirement is not possible this however means less accuracy on IMD measurement.

Rx linearity measurement: noise spec

We can apply the same reasoning as above for Rx linearity measurement. BB Bist send 2 tones to the Rx so that the level at Rx output is 5 dB below saturation (around -6dBv) to be in linear zone. Thus is reasonable to consider -16dBv/tone at VGAs output to be in the linear zone of VGA. The targeted spec to be measured is OIP3>4dBv. An extra margin of 14dB is taken to account for noise variance. Table below gives the noise level spec deduced for the baseband output for a linearity measurement at each gain of Rx:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| VGA gain | IF IIP3 [dBv] | Input level/tone [dBv] | input level (2 tones) [dBv] | atten | IM3[dBv] | Noise limit | Noise spec [dBv/sqrt(Hz)] |
| 25 | -21 | -41 | -35 | 12dB | -83 | -110 | -124 |
| 28 | -28 | -44 | -38 | 18dB | -100 | -127 | -141 |
| 31 | -31 | -47 | -41 | 18dB | -109 | -136 | -146 |
| 34 | -34 | -50 | -44 | 24dB | -118 | -145 | -155 |
| 37 | -37 | -53 | -47 | 24dB | -127 | -154 | -164 |
| 40 | -40 | -56 | -50 | 30dB | -136 | -163 | -173 |
| 43 | -43 | -59 | -53 | 30dB | -145 | -172 | -182 |
| 46 | -46 | -62 | -56 | 36dB | -154 | -181 | -191 |

Calculations shows that Rx linearity measurement is achievable only for lower gains (if 512samples are used in PDC). The noise specification for linearity measurement (at the lowest gain) with BB gain=0dB and atten=-12dB is -124dBv/sqrt(Hz).

*NOTA: after further investigations, noise the limiting factor for linearity will be ADC having SNR=60dB at 0dBFS and 40MHz BW. This means a noise density of -136dBv/sqrt(Hz). Most of linearity measurement cannot be done with only 512 samples. With this ADC noise we need up to 40M samples to observe the needed 70dBc free dynamic range. Which lead to the impossibility of measuring SFDR with this low input level.*

### Baseband implementation

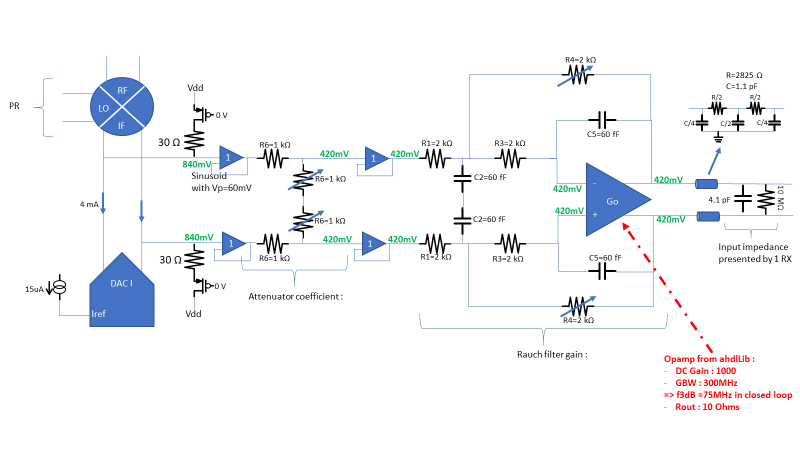


Figure 13: baseband block diagram

Signal at output of DAC :-20dBVp

Attenuation : 0-30dB by step of 6dB

Filter : Gain 0,6dB, 2nd order f3dB >75MHz

### BB filter trim:

* Implementation:

Rauch filter is intended to filter sigma delta quantification noise that have it’s maximum at 160MHz. on the other hand, the transfer function in the bandwith [0 40MHz] must not be affected by the filter (spec: level variation in the band <0.5dB).

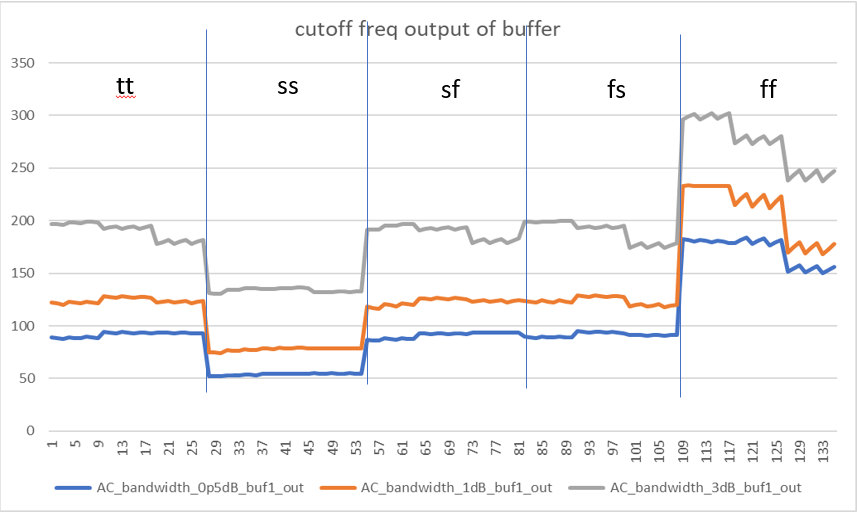
Figure below gives f-3dB and f-0.5dB of rauch filter over process:

Figure 13: rauch filter cutoff freq over corners and temp

For some corners f-3dB is up to 300MHz, for other corners f-0.5dB is as low as 50MHz. Thus some calibration is needed to achieve the right filtering without affecting the bandwidth, over corners.

This filtering does not have to be very accurate. The noise is not expected to cause any problems since it will be filtred by Rx filters. The goal is to remove as much noise as possible.

For these reasons the filter is only trimmed used extra capacitor bank. This trim at production is enough to reduce the cutoff frequency variation.

For that purpose, a bank of capacitors is added to allow trim of the cut off frequency to reduce it down to 50% of it’s nominal value.

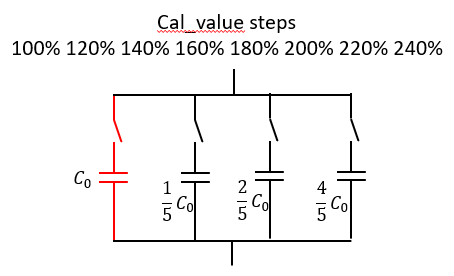


Figure 14: Capacitor banks implemented

* Trim method:

Trim of rauch filter will be done at room or at hot by measuring the attenuation of the filter at 50MHz. The capacitor value that gives the closest attenuation to -0.5dB at room, or -0.4dB at hot will be chosen as trim value. This ensure that the bandwidth 0MHz to 40MHz has less than 0.5dB attenuation while the cutoff freq is the lowest possible.

### Accuracy of the RFBIST measurement

There are different RS related to the RF bist. [artf1099953](https://doorsng.nxp.com/rm/resources/MB_b1dbc05eeab941a4b5e48bbefdccc9ac?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) [artf1098987](https://doorsng.nxp.com/rm/resources/_9d7cfd1d26c24ceb8ea07345bce60494?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) [artf1098984](https://doorsng.nxp.com/rm/resources/_d9a50e77e42b449488b654ef13a62fc4?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)

There are related to gain accuracy (leading to NF accuracy) and variation of the phase difference between channels. Indeed we can have an initial phase difference that will be calibrated by the customer in production but this phase measurement should remain constant with frequency.temperature,voltage and aging.

For that, some internal requirements are mandatory :

* Power detection must be accurate and close to the RX (to avoid variation of line loss). The level targeted is -10dBm diff/100ohm at Power detector input which is in the range of accuracy targeted by the power detector
* Coupler loss must be insensitive to load variation and to PVT (in the RX)
* Coupler phase mismatch must be insensitive to temperature, voltage, aging, frequencies (in the RX)

Error in Gain=error (PPD)+error(coupler)+error(fft)

Error in phase difference variation = error\_phasemismatch\_bistlines+error(fft)

### Accuracy of the BBBIST measurement

There are different RS related to the BB bist.

As the BB signal can be calibrated directly to the ADC. All other measurements are related to this (VGA gains, attenuation…) [artf1099896](https://doorsng.nxp.com/rm/resources/_6b203a966de24ce2b47f5e026a769ba2?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) [artf1098995](https://doorsng.nxp.com/rm/resources/_6d47ca4417e64d40b8ce1b39c6622049?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)

## Supplies

1LDO at 0.9V (doubler/DAC) and 1 LDO for 1.1V (IQ and buffers) 1LDO at 1.1V for BB

Each LDO can be disabled and by-passed separately. The bypass functionality is needed for voltage stress. Additionally, the output of each LDO will be accessible through the ATB for testing.

## DFT (from Benoit Poussard)

Ahead any functional/structural measurements, the LDOs have to be trimmed. The trim strategy is described in the Global bias chapter of the DfT AS.

The SCAN covers the digital parts of BiST IP as per DfX rules.

All buffers, mixers, PPD detectors, LDOs and PR will embedded accesses to key voltages. They are connected to the DC-ATB bus to be measured with the BiST-ADC. These voltages are defined with the designer to achieve the coverage in the order of magnitude of about 70% with DOTTS. At the time of writing, 04-June-2020, the schematic isn’t mature enough to define precisely these voltages.

The current consumptions of each sub-blocks are measured by delta method (overall current with the function ON versus OFF).

Intermediate PPD detectors in the RX BiST path are measured to assess of the SSB functionality. At Loout and SSB-out.

There is no analog resource for the mass production at the ATE. The IF generator signal magnitude and purity are measured at the ATE with the 8 RX ADC. This strategy is valid here from a test point of view because it is unrealistic that a defectivity affecting the magnitude of the BiST IF DAC can be fully compensated by 8 another defectivities on the 8 RX ADC”

The RX channel-to-channel phase measurement is limited by the RX path & SSB modulator image rejections. The image rejection cannot be measured at the ATE as assessed in this report : <https://www.collabnet.nxp.com/sf/go/doc414449?nav=1&pagenum=1&pagesize=15>.

The RX BiST has a power detector as close as possible of the LNA or mixer inputs. It is used as power reference to measure the RX conversion gain. The isolation of the coupler is a contributor of RX gain measurement uncertainty. It cannot be measured. It is taking into account in offsets between the DfT and the UDI RX gain measurement. The repeatability of this isolation is critical for the measurement accuracy. It will be evaluated thanks to the delta between the DfT and UDI measurement during the safe-launch phase. The repeatability limitation have to be taken into account in the RX gain/NF limit guardbands.

Some signals and internal nodes are sent to the ATB and used for the functional safety [[artf1200726,728,729](https://doorsng.nxp.com/rm/resources/_299397d8caf447798364aa655f7b7b90?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) ]:

2 LDO 1.1V

1 LDO 0.9V

* buffer2A:

VDD, copy of bias gate, copy of bias source current (between 0uA and 90uA)

* buffer2B/2C:

Vcasc, VDD, Copy of bias gate, copy of bias source current (between 0uA and 90uA)

* PR:

idac\_In/p, idac\_Qn/p, vdd\_pr\_1v1, vdd\_dac\_09, vss\_dac, Vss\_pr, Vbias\_pr\_gate, vssa\_dacbias\_1v45

* Doubler:

Vdiode\_sense\_amp40G, Vdiode\_sense\_amp80G, Vdiode\_sense\_doubler, Vbias\_doubler, vbias\_amp80\_diff, vdd\_sense\_doubler, vdd\_sense\_amp40. Iref\_amp40, Iref\_amp80, Iref\_doubler, ibias\_ppd\_20u\_bg, vgate\_cap\_ldo, res\_amp\_p, iref\_doubler\_img

* DAC:

TBD

* BB Bist:

90uA bias, Output Of the DAC n/p, output of the follower, Internal Vcm, output Vcm.

## Electrical specifications

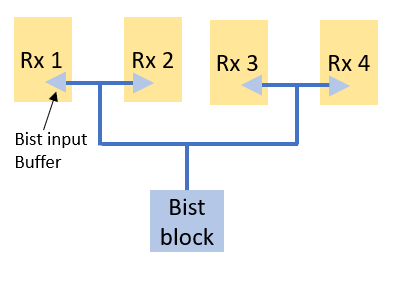
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | | | | min | typ | max |  | Test | Labo | Simu | Linked Doors RS | comment |
|  |  |  | Specification for the RF part | | | | | | | | | |
| LO input frequency | | | | 38 |  | 40.5 | GHz |  |  |  |  |  |
| Supply provided by LDO | | | | -7% | 0.9 | +7% | V |  |  |  |  | +/-5% full performance, +/-7% full fonctionality |
| Supply provided by LDO | | | | -7% | 1.1 | +7% | V |  |  |  |  |
| Safety supply | | | | -7 | 1.8V | +7% |  |  |  |  |  |
| Input LDO supply | | | | 1.45V-7% | 1.45V | 1.45V+7% | V |  |  |  |  |  |
| LO input level | | | | -12 |  |  |  |  |  |  |  |  |
| LO input level boost mode | | | | -10 |  |  |  |  |  |  |  |  |
| LO output level | | | | 2.5 |  |  | dBm |  |  |  |  | Calibrated through the PPD |
| RF output frequency | | | | 76 |  | 81 | GHz |  |  |  |  |  |
| SSB IR | | | | 20 |  |  | dB |  |  |  |  | [artf1098983](https://doorsng.nxp.com/rm/resources/_c743a068c8344f28aae9fb9bb5fb1e5d?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| SSB CR | | | | 20 |  |  | dB |  |  |  |  | [artf1098989](https://doorsng.nxp.com/rm/resources/_c743a068c8344f28aae9fb9bb5fb1e5d?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| SSB\_out max power  After calibration | | | | +4 |  |  | dBm |  |  |  |  | To measure accurately with the PPD detector at input coupler  [art1098992](https://doorsng.nxp.com/rm/resources/_756e326b06f1448d9a11ac0acaea7dc7?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| SSB\_out mx voltage after calibration | | | |  |  | 930 | mVpkd |  |  |  |  | To measure accurately with the PPD detector at buffers ouput |
| SSB\_out min power | | | |  |  | -20, tbf | dBm |  |  |  |  | To be able to measure the RF with min gain and max gain  [artf1100028](https://doorsng.nxp.com/rm/resources/MB_ebe21cdf7fef41e4bf9a9c6909d2609e?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Analog SSB out step power | | | |  |  | 3 | dB |  |  |  |  | [artf1100029](https://doorsng.nxp.com/rm/resources/MB_9aef492d61b9428594b3e6f129cb6bc7?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| SSB voltage at RX input | | | | 140 |  |  | mVpkd |  |  |  |  | Where the peak detector is (140mVpk power min for peak detector for +/-0.5 dB accuracy) |
| Phase difference variation between 4 SSB output (splitter output) over PVT must be | | | | -0.5 |  | 0.5 | deg |  |  |  |  |  |
| Linearity of buffer1 current DAC | | | |  |  | 1 | dB |  |  |  |  |  |
| Linearity of buffer2 current DAC | | | |  |  | 1 | dB |  |  |  |  |  |
| Linearity of buffer3 current DAC | | | |  |  | 1 | dB |  |  |  |  |  |
| Isolation between Rx channels when Bist is off | | | | 40dB |  |  |  |  |  |  |  | To guarantee he isolation between RX channels incl RX switches off |
| Phase/amplitude noise at SSB out (mode constant) | | | | -140-tbf |  |  | dBc/Hz |  |  |  |  | Can be discussed, need to be known |
| IF bandwidth | | | | 0.01 |  | 60 | MHz |  |  |  |  | Guarantee the gain over RX bw  [artf1098990](https://doorsng.nxp.com/rm/resources/_4d2dfbc51fb64ac79c654daa81f87044?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Return loss at splitter and transformer interfaces | | | |  |  | -10 | dB |  |  |  |  | This guaranties that PPD measured voltage is due to forward wave and not reflected wave |
| Should allow to power off the 3 buffers independently | | | |  |  |  |  |  |  |  |  |  |
| Specification for the DAC part | | | | | | | | | | | | |
| PRDAC Bias Current range | | | | 2 |  | 15 | uA |  |  |  |  | To allow RRF gain calibration and control |
| PRDAC bias current step | | | |  |  | 0.5 | uA |  |  |  |  | To allow RRF gain calibration and control |
| DAC current control linearity | | | |  |  | 1 | LSB |  |  |  |  | To allow the use of binary search algorithms for cal |
| INL PRDAC | | | |  | 0.3 | 0.5 | LSB |  |  |  |  |  |
| DNL PRDAC | | | |  | 0.03 | 0.06 | LSB |  |  |  |  |  |
| Thermometric DAC number of cells | | | |  |  | 256 |  |  |  |  |  |  |
| Specification for the BB part | | | | | | | | | | | | |
| IF bandwidth-1dB | | | | 0.01 |  | 60 | MHz |  |  |  |  | Guarantee the gain over RX bw  [artf1100138](https://doorsng.nxp.com/rm/resources/MB_cb5b5f4098c84cfa8760c42bcd9dd742?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Impedance to drive per channel | | | | 10.5 |  |  | Kohm |  |  |  |  |  |
| Spurious generation  range 1  [10K-40MHz] | | | | 70 |  |  | dBc |  |  |  |  | For aDC spurious  [artf1098998](https://doorsng.nxp.com/rm/resources/_d24e3d81fd1946af97e1635bdbc314a0?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| IMD3 2 tones  Range1 -6dB per tone  [10K-40MHz] | | | | 70 |  |  | dBc |  |  |  |  | For aDC spurious at 0dBFS |
| IMD2 2 tones  Range1 -6dB per tone  [10K-40MHz] | | | | 70 |  |  | dBc |  |  |  |  | For aDC spurious at 0dBFS |
| |  | | --- | | Bbout max level without Boost | |  | |  | | | | | |  |  | | --- | --- | | -22 | -20 | |  |  | |  | -56 | | -20 |  |  |  |  |  |  | dBV |
| Bbout max level with Boost mode (VGA gain=6) | | | | |  |  | | --- | --- | | -16 | -14 | | -14 |  |  |  |  |  |  | dBV |
| Bbout min level without Boost | | | | -58 | -56 | -55 |  |  |  |  |  | dBVpkdiff |
|  | | | |  |  |  |  |  |  |  |  |  |
| BB analog out step | | | |  |  | 6 | dB |  |  |  |  |  |
| Noise spectral density  [10K-40MHz] | | | |  |  | -149 | dBv/sqrt(Hz) |  |  |  |  | To be able to measure the SFDR with limited number of samples |
| BB analog out step | | | |  |  | 6 | dB |  |  |  |  |  |
| Attenuator range | | | | 0 |  | 36 | dB |  |  |  |  |  |
| BB out power variation over the frequency bandwidth (ripple) | | | | -0.25 |  | 0.25 | dB |  |  |  |  |  |
| Relative accuracy between vga1(or vga2) input path to adc test path | | | | -0.5 |  | 0.5 | dB |  |  |  |  | To measure the gain of receiver (receiver) |
| Relative phase difference between bb outputs | | | | -1 |  | +1 | deg |  |  |  |  |  |
| BB out step power (dig+ana) | | | |  | 0.5 |  | dB |  |  |  |  | For saturation detector +fine tune cordic  [artf1204917](https://doorsng.nxp.com/rm/resources/MB_a59b6780ecdf4bf4855da0595715f05b?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)  [artf1204911](https://doorsng.nxp.com/rm/resources/MB_e234d3d31a244f26829f18a5b4291538?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Analog control VGA | | | | -30 |  | 6 | dB |  |  |  |  |  |
| Analog step control | | | |  | 6 |  | dB |  |  |  |  |  |
| Attenuation of the rauch filter at 100MHz | | | | tbf |  |  | dB |  |  |  |  | 2nd order filter, should not impact at 40MHz |
| BB out power variation over the frequency bandwidth (ripple) | | | | -0.25 |  | 0.25 |  |  |  |  |  | [artf1153493](https://doorsng.nxp.com/rm/resources/MB_a9edbc218aa64d099897212542351238?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
|  | | | |  |  |  |  |  |  |  |  |  |
| Current consumption on 1.45V (incl LDO) | | | |  |  | tbf | mA |  |  |  |  |  |
| current consumption RXbist on LDO LO 0.9V RF mode | | | |  |  | 59 | mA |  |  |  |  |  |
| current consumption RXbist on LDO RF 1.1V RF mode | | | |  |  | 110 | mA |  |  |  |  | [artf1098960](https://doorsng.nxp.com/rm/resources/_aab08473c25a44e3991d0083e9bfc01f?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| currentconsumption bbbist on LDO BB 0.9 V  BB mode | | | |  |  | 30 | mA |  |  |  |  | [artf1098959](https://doorsng.nxp.com/rm/resources/_78cb3b0b306544fca7712c258a0c9238?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Current consumption on LDO dig 0.9V | | | |  |  | 5 | mA |  |  |  |  |  |
| Powerdown current rXbist,bbbist (1.45V) | | | |  |  | 500 | uA |  |  |  |  | [artf1204771](https://doorsng.nxp.com/rm/resources/MB_58adc2faa41b4ac8adccdbb414aa675f?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)  [artf1204774](https://doorsng.nxp.com/rm/resources/MB_58adc2faa41b4ac8adccdbb414aa675f?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Powerdown current rXbist,bbbist (1.8V) | | | |  |  | 100 | uA |  |  |  |  | [artf1204771](https://doorsng.nxp.com/rm/resources/MB_58adc2faa41b4ac8adccdbb414aa675f?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)  [artf1204774](https://doorsng.nxp.com/rm/resources/MB_58adc2faa41b4ac8adccdbb414aa675f?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Startup time/powerdon | | | |  |  | 1 | us |  |  |  |  | From poweron to signal out  [artf1204723](https://doorsng.nxp.com/rm/resources/_a1605403c25f48f0b3de45f1dfeb31d4?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Silcon area bb+ rf bist | | | |  |  |  |  |  |  |  |  |  |

Table 9: Electrical specification RXbist

Impedance to drive for the baseband buffer to RX :

The buffer will drive one long line that split to 4 lines to the Rx (Figure 9). The high capacitance load of the Rx (2.1pF to 6.3 pF) create with the parasitic resistance of the long lines (200Ohms best case) a pole at few Mhz reducing the signal BW. To increase this BW, a buffer with low input capacitance (<1.5pF) is put at the end of the lines in Rx side.

Figure 14: Bist to Rx lines



1

2

3

The equivalent model for those line is as follow. The line is devided into 3 parts for this model as shown in figure above. The values of parasitic resistance and capacitance of each part have been estimated by the layout team. Figure below show the values.

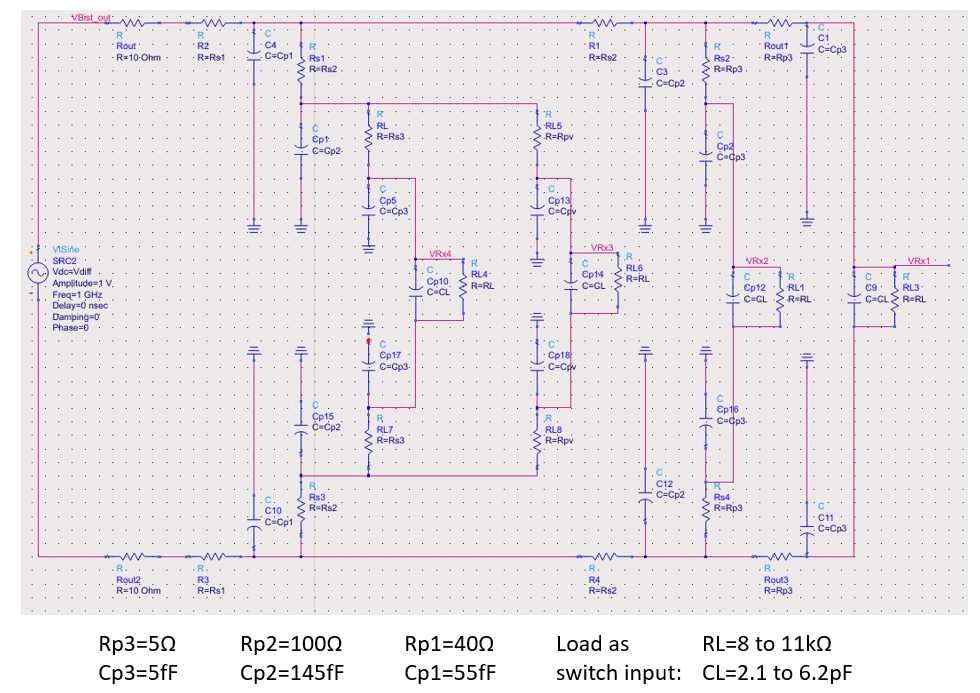


Figure 15: load impedance for bb bist

## Layout

Layout must fit in the floorplan

## Design Decisions (logged in DOORS AS)

|  |
| --- |
| RXBIST |
| RX bist is splitted between RF and baseband BIST (RXRFBIST and BBBIST). They are both controlled by a digital controller (RXDIG) |
| Bist digital generation can provide square wave, sine wave, 2 tones. |
| The RXDIG is generating pure sine wave based on sigma delta |
| RXDIG can control frequency,phase, amplitude and compensate for phase/amplitude unbalance |
| The Sigma delta is running at 320MHz from an external analog clock |
| A dynamic element matching is spreading the INL/DNL of the analog DACs |
| The RXDIG is able to provide 2 independent sine waves tones based on 2 cordics |
| IF frequency is programmable. Phase and amplitudes are programmables independentely for I and Q |
| The RXDIG provides I and Q signal |
| 2 8b DACs are used to convert the I,Q digital signals |
| These analog signals are used both for RXRFBIST and BBBIST |
| IF signal are converted in RF+IF through a SSB demodulator |
| The sSB demodulator is not compensated for image rejection because of the IQ receivers |
| The SSB signal is splitted and sent to reach receiver (LNA input or LNA output depending on the switch configuration inside the receiver) |
| The level of the IF signal can be controlled by the RF buffers, the PR current and the digital I,Q controls |
| The level at the SSB output is calibrated so that the PPD at rX inputs are in a accurate power range for reference measurement |
| The dynamic range in the SSB modulator allows measurement of all parameters through RF path with all VGA gains without compressing the VGA's. Linearity is only possible in Baseband mode |
| The BBBist has a programmable output levels. Attenuator and IF amplifiers are used after the DAC current to voltage conversion |
| BBBist is providing 2 filtered signals to filter the sigma delta high frequency noise |
| BBBist is able to drive the line between Bist and receiver inputs |
| Signals are post processed in software to determine the characteristics of the receivers. Also it is used to calibrate the IF signals |
| The following functions can be measured after postprocessing : RX RF gain, RX RF phase difference, NF, RX baseband gain and linearity, AGC gains, HPF and LPF, linearity of ADC |
| Any value outside software threshold range must create an error by the safety software |

# RXBIST Digital

## Block diagram

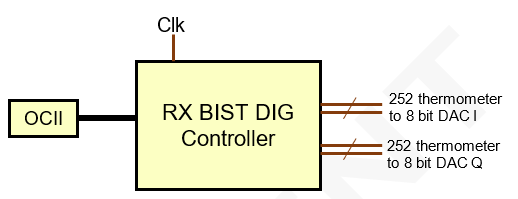


Figure 16: Simplified block diagram

This block generates I/Q digital signals to the 8-bit DAC I and Q to generate all BIST signal needed. This Output is be 256 thermometer coded bus for each DAC to allow individual control of each DAC cell.

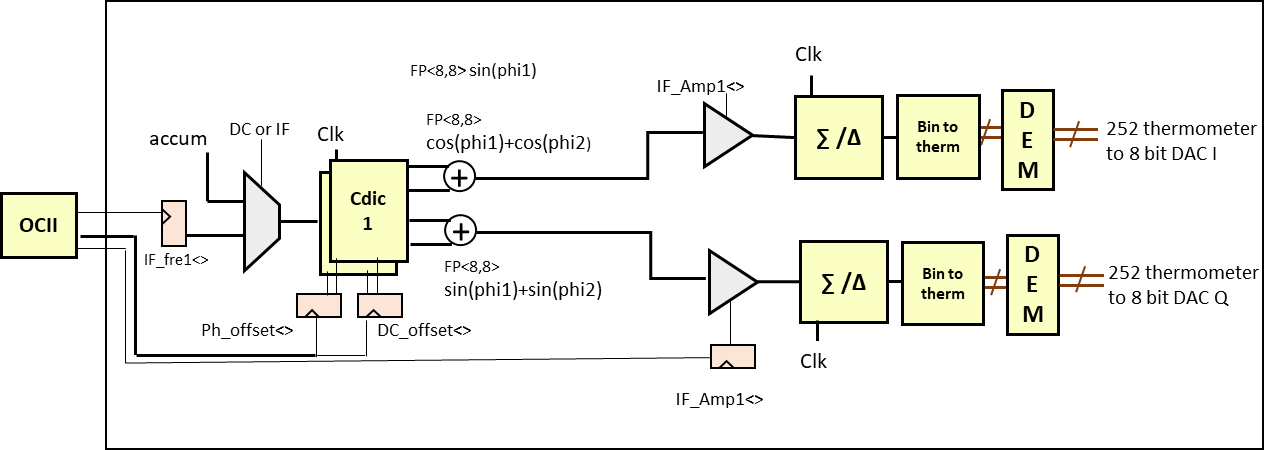
Digital module and registers will be configured and controlled through OCII access via ARM 7.

Figure 17: Bist digital block diagram

## General Functionality and Operational mode (to be updated)

It is possible to control independently the power on/off of the analog blocks :

4 modes of operation :

**Double CW:** Cordic 1 and 2 are used to generate 1 or 2 sinewaves I and Q with chosen frequencies at a sampling rate of 320MHz.Those sinewaves are added together with maximum half full-scale amplitude for each. 16 bits precision along with sigma-delta and DEM is enough to achieve the requirement in terms of SNR and SFDR as the bottleneck will be the 8-bit DAC.

**Square wave:** Cordic 1 and 2 are used to create square wave of I and Q to have multitone signal for filter testing. There is also a possibility to mix 2 square waves at 2 different frequencies.

**DC Controled:** this mode is to generate a DC level

**DAC test mode** : This mode allows the individual control of each DAC cell for measuring INL/DNL of the DACs. There is a mode where each N/P cell is enabled individualy using register (DC\_offset). And another model where the cells are automatically swept with a controllable period to allow fast INL/DNL measurement. Implementation details can be found in this document.

|  |  |
| --- | --- |
| Bist\_if\_mode<2:0> | 0:double CW  1:double square wave  2:DC controlled  3:DAC test mode |
| if1\_freq<15:0> | Frequency programmation cw1 (FP6.10) |
| if2\_freq<15:0> | Frequency programmation cw2  (FP6.10) |
| IF1\_amp<13:0> | Amplitude programmation cw1 |
| IF2\_amp<13:0> | Amplitude programmation cw2 |
| DC\_offset\_I<15:0> | Dc offset for the I |
| DC\_offset\_Q<15:0> | Dc offset for the Q |
| IF1\_<9::0> | Phase offset between I and Q |
| If1\_ph\_init<8:0> | Initial phase for tone 1 |
| If2\_ph\_init<8:0> | Initial phase for tone 2 |
| bypass\_sd | Bypassing of sigma delta |
| Bypass\_dem | Bypassing DEM |
| If1\_iqcomp\_gain | IF1 IQ gain compensation |
| If2\_iqcomp\_gain | IF2 IQ gain compensation |
| If1\_iqcomp\_phase | IF1 IQ phase compensation |
| If2\_iqcomp\_phase | IF1 IQ phase compensation |
| Trig\_source | Select start by trigstart signal or SPI (start\_mod) |
| Trig\_start | Start modulation when Trig\_start=1 (trig\_source=0) |
| Trig\_stop | When 1 stop the modulation |

Table 10 Digital RX control registers

When the trig signal rising edge occurs, the generation of the waves start. It is stopped when the trig\_stop is set to 1. At each trig start rising edge the phase is reseted. Trigstart signal is connected to chirp\_start of TE. If trigstart\_sel=1 the start of the modulation is controlled by trigstop register bit

## Description of the block

All blocks are driven by 320MHz clock.

The block is composed of :

* 2 accumulators that computes the phases for each clock step. Two are needed to generate two sine waves for dual tone mode.
* Digital square wave generator
* Programable gain block that scale the signal (amplitude and offset) to the desired amplitude.
* Sigma Delta modulator described in section
* Converter block from binary to thermometric output
* DEM block to transform the binary input word to thermometer coded, with a randomization of the on cells. This is needed for a good SFDR
* An IQ compensation circuitry to add offset, phase and gain offset (manual IQ calibration)

### Frequency control

Frequency is set in MHz. Registers have 16 bits precision in fixed point 6.10.

Fmax= 64MHz; Fmin=0; Fstep=1kHz

Although, for postprocessing reasons, Frequency must be chosen to fall in bin of fft when processed. It must follow the following formula:

Where in and integer, fft size chosen for postprocessing, sampling frequency of the ADC after decimation.

For a given fft size and frequency sampling, the minimum frequency F\_IF that can be chosen is

Table below gives minimum frequency allowed for few fft size/Frequency sampling

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Lowest programmable frequency [kHz] | | | | |
|  | Fs=10M | Fs=20M | Fs=40M | Fs=80M |
| FFT\_size=16 | 625 | 1250 | 2500 | 5000 |
| FFT\_size=32 | 312,5 | 625 | 1250 | 2500 |
| FFT\_size=64 | 156,25 | 312,5 | 625 | 1250 |
| FFT\_size=128 | 78,125 | 156,25 | 312,5 | 625 |
| FFT\_size=256 | 39,0625 | 78,125 | 156,25 | 312,5 |
| FFT\_size=1024 | 9,765625 | 19,53125 | 39,0625 | 78,125 |
| FFT\_size=2048 | 4,882813 | 9,765625 | 19,53125 | 39,0625 |

Table 11 Programmable frequencies

### Amplitude control

Amplitude is set in 8 bit register. This size allows to fine tune the amplitude with less than 0.1dB step.

### Cordic

Cordic is a digital calculator that computes Cosine and sine of the input phase. This block is driven by 320MHz clock to be at the same rate as sigma delta.

### Square wave generator

Generates two square wave functions in the same frequency but with a given phase difference.

### Sigma-Delta modulator

In order to achieve a good SNR/SFDR for the generated tone, a sigma-delta modulator is used to mash the fractional part of the tone generated by the cordic.

The following Block diagram shows the model used to validate the architecture in ADS:

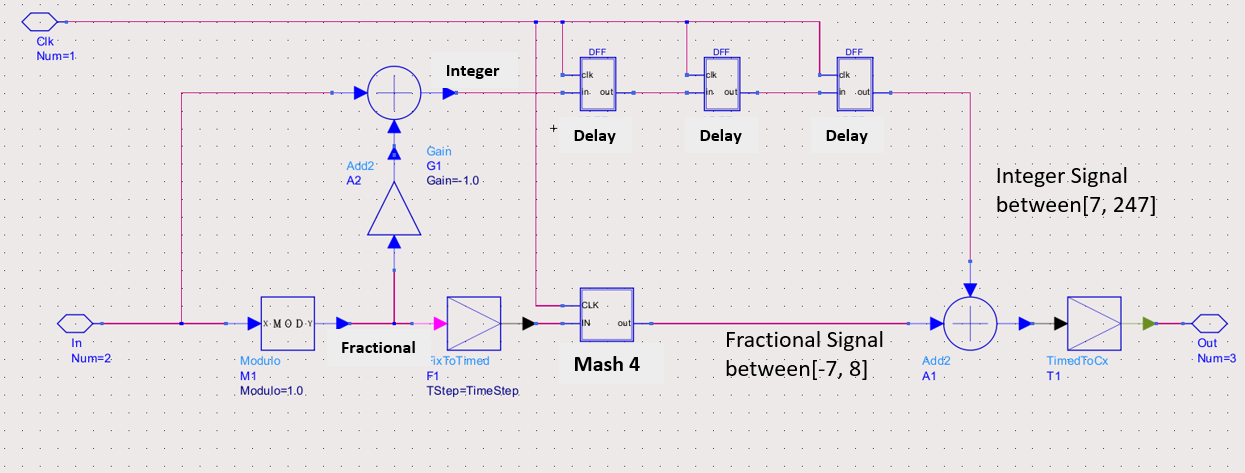


Figure 18: block diagram SD

As for PLL Sigma-Delta, Fractional part for the input signal is mashed while integer part is delayed to be added to fractional part. Studies show that clock around 320MHz is needed to achieve the SNR/SFDR requirement.

### Binary to unary conversion

This block converts 8-bit binary input from sigma-delta to a 256 unary (thermometer coded) that is meant to feed the DEM input or 8-bit thermometer coded DAC input when DEM is bypass. Chec jf levels offset compatibility with analog

### Dynamic element matching (DEM)

#### Introduction

MULTIBIT delta-sigma (ΔΣ) digital-to-analog converters (DACs) suffer from device mismatches that arise from layout parasitics and process nonidealities, such as gradient errors and random etching effects. The mismatch error, not shaped by the ΔΣ loop, causes severe linearity degradations. A way to address this issue is to use analog or digital calibration [1]–[3]. Another way is to use dynamic element matching (DEM) techniques [4]–[10]. A widely used DEM technique is to randomly scramble the element selection, which effectively turns the mismatch-induced distortion into white noise [4]. Another popular technique is data-weighted averaging (DWA) [5], [6], which does a first-order shaping of the mismatch error. Recently, more advanced techniques have been developed that can shape the mismatch errors to higher orders [7]–[10]. DEM based approaches do not need any prior knowledge of the device mismatch unlike calibration techniques [1]–[3]. This greatly reduces the design complexity, because the accurate measurement of DAC element mismatch is nontrivial.

Aside from the static mismatch, another major source for distortion in a continuous-time (CT) multibit ΔΣ DAC is inter-symbol interference (ISI), which represents the dynamic error during the switching of the DAC elements. It can be caused by asymmetric on-and-off switching, clock skew, cross-talk and parasitic memory effects. Unlike the element mismatch error that shows up only in multibit DACs, ISI error exists even in a binary DAC. An analog approach to reduce the ISI error is to use the return-to-zero (RZ) scheme [11]. However, RZ signaling is highly sensitive to clock jitter and has large output discontinuities leading to increased high-frequency content in the output.

Since the DEM techniques can randomize the DAC element selection, it might seem that they could somehow mitigate the ISI problem. Unfortunately, most existing DEM techniques (e.g., [4]–[10]) actually aggravate the ISI error. This is because most DEM techniques increase the DAC element transition rate in order to quickly randomize the selection pattern, thus increasing the ISI error. The popular DWA technique has the highest switching activity and produces the largest ISI error. Recently, two novel digital techniques have been developed that can mitigate ISI errors [12], [13]. The key idea of [12] is to maintain the total number of up (0 → 1) and down (1 → 0) transitions of all DAC elements at a constant level independent from the input, thus turning the majority of ISI error into an offset. The technique in [13] ensures the long-term average of the DAC transition rate is kept constant, thus high-pass shaping the ISI error. Nevertheless, [13] has two drawbacks: 1) its implementation is relatively complicated; and 2) its second-order distortion increases rapidly with the input amplitude. Thus, to ensure a good distortion performance, the maximum input signal amplitude is limited to −6 dBFS, which is undesirable.

Despite its simplicity, thermometer coding has the lowest transition rate, and thus has the smallest ISI error. Element transition in thermometer coding is mainly dictated by random quantization noise, thus resulting in low ISI-induced distortion.

The main drawback for thermometer coding is static mismatch issue. Recently, researchers have developed a modified thermometer coding scheme that has the same transition activity as thermometer coding but can whiten the mismatch error [14]. However, it cannot shape the mismatch error, and hence, the in-band low-frequency mismatch error is still large and limits the DAC performance.

#### DEM Algorithm Description

The input of the DEM is signal **s**, which is an integer number ranging from 0 to N that indicates the number of outputs bit to be asserted. The output consist of a vector of N bits. In case of RXBist, N = 252.

The block diagram of the DEM is depicted in Fig 1. It consists of:

* **Output registers**, which hold the current output,
* **Decoders**, one for each output register,
* **Pointer Logic**, which generates the points idx\_begin and idx\_end, the signal s’ which holds the number of outputs to be asserted,
* **Boost and Shuffle Control**, for realizing constant performance
* **Spread-spectrum Control**, for shaping the spectrum

|  |
| --- |
|  |
| 1. DEM Block diagram |

The Pointer-Logic translates the current input level, s, into the appropriate levels of *idx\_begin* and *idx\_end*, for asserting or de-asserting bits in the output vector. Initially, when *idx\_begin* ≤ *idx\_end*, the asserted output bits range from *idx\_begin* to *idx\_end* as depicted in Fig 2.

|  |
| --- |
|  |
| 1. Simplified view of the DAC elements being asserted |

When *idx\_begin* and *idx\_end* are equal, either all or none of the output bits are asserted. In such a case, signal s’ indicates the number of bits that must be asserted: if 0, none is asserted; if *N*, all are asserted.

Note that, *idx\_end* is not pointing to the last bit being asserted, but it is pointing to the first one NOT being asserted. After some time, explained in Section 2.1, the pointers can also be in reverse order (meaning *idx\_begin* ≥ *idx\_end*) as depicted in Fig 3. Then, the asserted bits range from *idx\_begin* to 251, and from 0 to *idx\_end-1*.

|  |
| --- |
|  |
| 1. Asserted elements in case the pointers are in reverse order |

In the next sections, the various modules are explained in more detail.

#### Pointer Logic

The pointer logic updates the pointers as a function of *s*. It does so by computing the difference, *d*, compared to the previous input:

*d(i)* = *s*(i) – *s*(i-1)

If *d* is positive, *idx\_begin* is incremented with *d*. If *d* is negative, *idx\_end* is incremented with -*d*. If d is zero, *idx\_begin* and *idx\_end* remain constant.

Given this scheme, (1) the number of output transitions (corresponding to enabling/disabling of unit-elements) is minimal while (2) the unit elements are equally used over time due the principle of “recycling”.

The advancing of the pointers *idx\_begin* and *idx\_end* is depicted in Fig 4 for a noise-shaped sine-wave signal.

|  |
| --- |
|  |
| 1. Advancing of the *begin* and *end* pointers for a sine-wave signal |

Since the latency of the DEM is not constrained by a requirement, the pointer-logic function may have one (or a couple of) clock cycles delay.

#### Unit element grouping

For realizing better performance while maintaining these two properties, a scheme with “grouping” of the unit-elements is added on top of this pointer scheme.

|  |
| --- |
|  |
| 1. Grouping with groups-size = 2 |

In Fig 5, grouping with group-size = 2 is illustrated, where the groups are indicated by the green boxes. The effect of grouping is that when the pointers (begin / end) are advancing, only 1 unit element per group is enabled / disabled. So, with group-size = 2, it means that 2 passes are required to enable (disable) all unit elements. In general, with group-size = *g*, it takes *g* passes to enable (disable) all unit elements. The enabling (disabling) in each group is done (pseudo) randomly. Hence, the combination of enabled cells is different for each subsequent pass of the pointers. This form of randomization does not come at the cost of additional transitions, so the SNDR and SFDR performance will improve unconditionally. The larger the group-size, the better the performance will be. However the implementation of a larger-group size results in a more complex implementation. For this reason for RX BIST we have chosen for the implementation of group-size = 2.

#### Derivative Control

The pointer logic enables and disables the unit-elements of the DAC as function of the input level of the DEM. Consequently, for IF tones with low(er) frequency or low(er) amplitude, less unit-elements will be (de-)asserted per unit time which results in less SFDR performance. To overcome this issue, a BOOST concept has be implemented as depicted in the block-diagram (see Fig 1). Here, the signal BST is a natural number which defines the number of unit-elements that is re-cycled per clock period in addition to the re-cycling due to the signal variation. In terms of the pointers *idx\_begin / idx\_end* this means:

idx\_begin := idx\_begin + BST

idx\_end := idx\_end + BST

If *BST* = 0, this feature does not change the pointers, if *BST* > 0 the re-cycling of unit-elements is increased by *BST* unit-elements per clock period.

To realize sufficient (a minimal amount of) re-cycling per unit of time, signal *BST* is derived from the input as follows:

*BST* = floor(**D\_FAC**\*max(0,**D\_MIN**-abs(*d*))\*rand())

where rand() is a Matlab function which generates random numbers in the range [0,1> drawn from an uniform distribution, **D\_FAC** and **D\_MIN** are parameters, and *d* is the difference between the current and the previous input level.

The number of extra transitions caused by the BOOST technique equals: 2\**BST*. Hence, the expected (average) number of transitions as function of abs(*d*) is:

E(transitions) = **D\_FAC**\***D\_MIN** + (1-**D\_FAC**)\*abs(*d*), if abs(*d*) < **D\_MIN**

E(transitions) = abs(*d*), if abs(*d*) ≥ **D\_MIN**

|  |
| --- |
|  |
| 1. Average number of transitions as a function abs(*d*) due to BOOST control |

#### Spread-Spectrum Control

The RX BIST IF tones are pure sine-waves, so periodic of nature. Consequently, the pointers *idx\_begin* and *idx\_end* will advance and wrap in correspondence with the amplitude[[2]](#footnote-2) and frequency of the IF tone. The periodic correlation between the IF tone and the wrapping of the pointers causes spurs which deteriorates the SFDR performance. To prevent/mitigate this problem, a spread-spectrum technique is used which distributes the energy of the systematic spurs over a range of frequencies which makes the worst case spur energy lower.

To that end, the wrap frequency of the pointers is modulated by applying a BOOST level every clock cycle which is randomly updated every couple of pointer wrappings:

*ss\_bst\_r* = **SS\_L**\*rand()

In here **SS\_L** is a parameter which specifies the maximum possible boost level. To minimize the number of transitions, the boost levels are chosen relatively small: **SS\_L** is in the range from 4 … 7. As *ss\_bst\_r* is a real (none integer) number, the conversion into integer boost levels is as follows:

ss\_bst = round(ss\_accu);

ss\_accu = ss\_accu + (ss\_bst\_r - ss\_bst);

in here, *ss\_bst* and *ss\_bst\_r* are on average equal.

The boost level updating is performed after **SS\_C** or **SS\_C**-1 wrappings of *idx\_begin* and/or *idx\_end.*

#### Shuffle Control

Both Derivative Control and Spread-Spectrum Control rely on the BOOST technique. This technique works fine for small and larger signal levels. Close to 50%, BOOSTING is however not effective. This is because, a BOOST has only effect in case the number of enabled cells in the groups changes e.g. from 0 to 1. If all groups have 1 of the 2 cells enabled (this is for s=50%), a BOOST, small or large, has does not result in asserting of de-asserting of cells. Hence we need an alternative technique to cope with this situation.

This technique is called “Shuffle Control”. In here, all of the groups of 2 cells with exactly 1 cell enabled, will be updated in 6 interleaved sets as depicted in Fig 7.

|  |
| --- |
|  |
| 1. Shuffle control updates the groups of 2 in 6 interleaved sets |

The 6 sets are updated, one after the other in a round-robin fashion, in subsequent clock cycles with a probability as depicted in Fig 8. If a set is updated, the next set is targeted in the next clock cycle. If a set is not updated (due to the probability mechanism), the same set is targeted again in the next clock cycle.

|  |
| --- |
|  |
| 1. Probability distribution as function of the relative signal level |

Updating of a set means that all its “groups of 2 cells” with exactly 1 cell enabled, get randomly a new cell enabled.

**REMARK**: If the Shuffle operation is applied, the BOOST operation from the Derivative control is skipped. In this way the number of transitions per clock-cycle is kept minimal.

#### Parameter overview

1. DEM Settings

| Parameter | Range | Default | Description |
| --- | --- | --- | --- |
| D\_MIN | 14 … 28, step 2 | 20 | Threshold for Derivative Control |
| D\_FAC | 1.0 ... 2.5, step ½ | 2.5 | Factor for Derivative Control |
| SS\_C | 4 … 7 | 5 | Spread-spectrum update interval (in # pointer wrappings) |
| SS\_L | 3.5 … 7.0, step ½ | 5.0 | Spread-spectrum max boost level |
| SH\_P | 0.25 … 0.40,  step 0.05 | 0.35 | Shuffle Control probability parameter |

#### Performance Figures

FFT-size = 4096, #Unit-elements = 252

Unit element parameters: Std-dev = 0.014, max-skew = 75ps

|  |
| --- |
|  |
| 1. Performance for “grouping by 2”, without Derivative, Shuffle and SS Control |

With Derivative Control DF=2.5

|  |
| --- |
|  |
| 1. Performance for “grouping by 2”, D\_F=2.5, SH\_P=0, SS\_L=0 |

With Derivative Control DF=1

|  |
| --- |
|  |
| 1. Performance for “grouping by 2”, D\_F=1.0, SH\_P=0, SS\_L=0 |

With Shuffle Control

|  |
| --- |
|  |
| 1. Performance for “grouping by 2”, D\_F=0, SH\_P=0.35, SS\_L=0 |

With Spread-Spectrum Control

|  |
| --- |
|  |
| 1. Performance for “grouping by 2”, D\_F=0, SH\_P=0, SS\_L=5.0 |

With Derivative, Shuffle and Spread-Spectrum Control

|  |
| --- |
|  |
| 1. Performance for “grouping by 2”, D\_F=2.5, SH\_P=0.35, SS\_L=5.0 |

## Interface

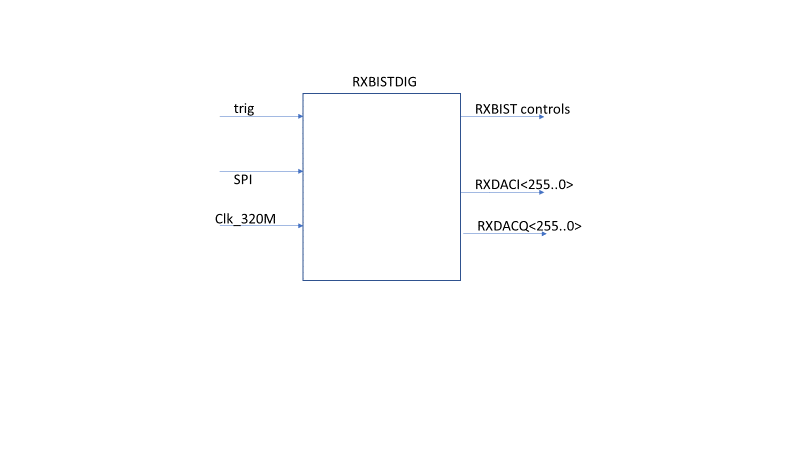


Figure 33: RXBIST digital

|  |  |  |  |
| --- | --- | --- | --- |
| I/O | interface | type | definition |
| sclk, | dig/dig | in | spi |
| Ss\_n | dig/dig | in | spi |
| mosi | dig/dig | in | spi |
| miso | dig/dig | out | spi |
| Rst\_an | dig/dig | in | reset |
| Clk\_320m | dig/dig | in | clock |
| Trig\_start | Dig/dig | in | Start of trig (from TE) |
| Enable\_rxbist | Dig/dig | in | General enable of the bist from TE |
| Fast\_en | Dig/dig | in | General fast enable from TE |
| Rx\_daci | Dig/ana | Out<251:0> | Control of DAC |
| Rx\_dacq | Dig/ana | Out<251:0> | Control of DAC |
| Pon\_ls\_rxbist | Dig/ana | out | Control LS analog |
| Pon\_ldo\_rxbist | Dig/ana | Out<3:0> | Control LDO |
| Enable\_rxbist | Dig/ana | Out<7:0> | Control enables |
| Fast\_enable | Dig/ana | out | Fast enable |
|  |  |  |  |
| Gain\_BB\_buffer <2:0..> | Dig/ana | out |  |
| BB\_atten <..> | Dig/ana | out |  |
| DAC\_current<4:0> | Dig/ana | out |  |
| Gain\_buffer1<5:0> | Dig/ana | out |  |
| Gain\_buffer2<5:0> | Dig/ana | out |  |
| Gain\_buffer3<5:0> | Dig/ana | out |  |
| Atb\_bus1<.> | Dig/ana | out |  |
| Atb\_bus2 | Dig/ana |  |  |
| LO\_bias<3:0> | Dig/ana | out |  |
| Bistrx\_mode | Dig/ana | out |  |
|  |  |  |  |

Controls (on/off) of the analog are described in 4.2

## Electrical specifications

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| spec | min | typ | max |  | Linked Doors RS | comment |  |
| Max time for safety |  |  | 4ms-Tcal | ms | yes | Should be in the total safety budget | [artf1098986](https://doorsng.nxp.com/rm/resources/_1158faa31334446ab92e0b2f1a5baf43?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Clock frequency |  | 320 |  | MHz |  |  |  |
|  |  |  |  |  |  |  |  |
| Gain resolution |  | 0.1 | 0.5 | dB |  | For DFT | [artf1099953](https://doorsng.nxp.com/rm/resources/MB_b1dbc05eeab941a4b5e48bbefdccc9ac?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Phase resolution |  | 0.005 | 0.1 | deg |  | For DFT | [artf1098987](https://doorsng.nxp.com/rm/resources/_9d7cfd1d26c24ceb8ea07345bce60494?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) 360/2^16 |
| IF resolution | 1 |  |  | KHz |  | For DFT | [artf1098984](https://doorsng.nxp.com/rm/resources/_d9a50e77e42b449488b654ef13a62fc4?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)  [artf1098988](https://doorsng.nxp.com/rm/resources/_9e68fb4b793e4edc99399dd80ee95f47?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| SFDR after DEM at Full scale | 70 | 80 |  | dBc |  |  |  |
| SNR at full scale | tbf | 60 |  |  |  |  |  |
| Amplitude range | -30 |  | 0 | dBFS |  |  |  |
|  |  |  |  |  |  |  |  |
| Gain compensation between I,Q range | 0 |  | 5 | dB |  |  |  |
| Gain compensation between I,Q resolution |  | 0.2 |  |  |  |  |  |
| Phase compensation between I,Q | 0 |  | 4 | deg |  |  |  |
| Phase compensation between I,Q resolution |  | 0.5 |  |  |  |  |  |
| IF frequency | 0.01 |  | 60 | MHz |  |  |  |
| Dynamic out |  | 252 |  | bits |  |  |  |
| delay mismatch |  |  | 75 | ps |  |  |  |
| area |  |  | tbf |  |  |  |  |

Table 12: electrical spec RXbist digital

## Calibration of the RFbist

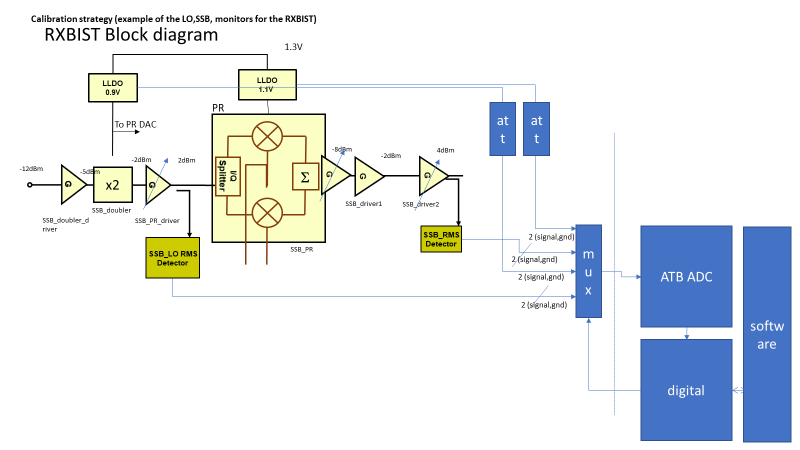


Figure 34 Bist calibration/saftey implementation

The calibration mechanism is based on a software approach.

The power detector analog output can be sent to ATB. They are converted in digital and processed by software). It is used for

* Calibrating the doubler output power to get the 2.5dBm
* Calibrating the SSB modulator to get the correct output power 4dBm

See Post processing with ARM and software (calibration and safety)

## Design Decisions (to be logged in DOORS AS)

|  |
| --- |
| RXBIST |
| RX bist is splitted between RF and baseband BIST (RXRFBIST and BBBIST). They are both controlled by a digital controller (RXDIG) |
| Bist digital generation can provide square wave, sine wave, 2 tones. |
| The RXDIG is generating pure sine wave based on sigma delta |
| RXDIG can control frequency,phase, amplitude and compensate for phase/amplitude unbalance |
| The Sigma delta is running at 320MHz from an external analog clock |
| A dynamic element matching is spreading the INL/DNL of the analog DACs |
| The RXDIG is able to provide 2 independent sine waves tones based on 2 cordics |
| IF frequency is programmable. Phase and amplitudes are programmable independently for I and Q |
| The RXDIG provides I and Q signal |
| 2 8b DACs are used to convert the I,Q digital signals |
| These analog signals are used both for RXRFBIST and BBBIST |
| IF signal are converted in RF+IF through a SSB demodulator |
| The sSB demodulator is not compensated for image rejection because of the IQ receivers |
| The SSB signal is splitted and sent to reach receiver (LNA input or LNA output depending on the switch configuration inside the receiver) |
| The level of the IF signal can be controlled by the RF buffers, the PR current and the digital I,Q controls |
| The level at the SSB output is calibrated so that the PPD at RX inputs are in a accurate power range for reference measurement |
| The dynamic range in the SSB modulator allows measurement of all parameters through RF path with all VGA gains without compressing the VGA's. Linearity is only possible in Baseband mode |
| The BBBist has a programmable output levels. Attenuator and IF amplifiers are used after the DAC current to voltage conversion |
| BBBist is providing 2 filtered signals to filter the sigma delta high frequency noise |
| BBBist is able to drive the line between Bist and receiver inputs |
| Signals are post processed in software to determine the caracteristics of the receivers. Also it is used to calibrate the IF signals |
| The following functions can be measured after postprocessing : RX RF gain, RX RF phase difference, NF, RX baseband gain and linearity, AGC gains, HPF and LPF, linearity of ADC |
| Any value outside software threshold range must create an error by the safety software |

# TXBIST Analog

## Block diagram

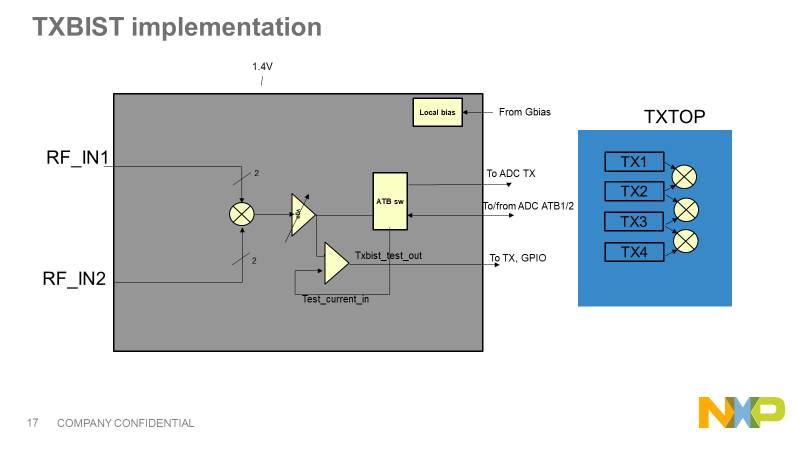
In this AS is detailed the phase measurement between channels system and also the phase step measurement (used in the safety). The block is used 3 times in the 4TX module and is controlled by the TXdig in the TX.

Figure 35: TXbist implementation

## General Functionality and Operational mode

### operational mode

The TXBIST allows to measure the phase difference between 2 TXchannels. It is placed between 2TX channels. There are 3 txbist in the chip.

On top of that there are some power detectors along the TX chain, especially at the power output (see Figure 16) [[artf10989973 and 1098970](https://doorsng.nxp.com/rm/resources/_b1eee43dafdf4213864aeac5465e1c05?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)].[[artf1098964](https://doorsng.nxp.com/rm/resources/_01072057bd074da19bda71e71999c866?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136)]

The analog information is sent to the ATB ADC through a mux. LDO output and TX/TX phase difference can be sent to the ATB bus or ADC TX

Different mode of operations :

* Phase difference variation between channels (safety) : the initial phase between channels is not specified (calibrated in production by the customer). Measuring the phase difference between channels and keeping this information in memory allow to generate a reference. Measuring the difference in safety and comparing to the reference allow to track the variation due to aging, frequency, temperature, supply. The variation due to frequency,temperature and supply is guaranteed
* Phase steps measurement. Phase step is defined as the difference of phases between 2 successive phases of 1 TX channel.
* Phase init measurement. This is the absolute phase difference between 2 channels.

The accuracy of the phase measurement depends on the power at the output of the PA, but also depends on error introduced by the TXBIST. Others parameters such as the phase rotator INL are impacting the phase step measurement, The repeatability of the phase rotator calibration can impact the accuracy of the TX 2 TX delta phase variation.

### Power modes

From the outside there are 4 main digital signals that control the IP functional states. These states are described in Table 4.

|  |  |  |
| --- | --- | --- |
| State | Note | Controls |
| Off | The lowest power state. Everything is off. The pon\_ls\_txbist is forcing all signals to analog block to 0. | pon\_ldo\_txbist=x  pon\_ls\_txbist=0  en\_txbist=x  fast\_enable\_txbist=X |
| Standby | Ldo “enable” are activated but LDO are off | pon\_ldo\_txbist=0  pon\_ls\_txbist=1  en\_txbist=x  fast\_enable\_txbist=X |
| Standby2 | LDO are turned on | pon\_ldo\_txbist=1  pon\_ls\_txbist=1  en\_txbist=x  fast\_enable\_txbist=X |
| Fast turn on | Transition state between the standby and on states. The fast\_enable is high, which shorts the R in the bias RC filters to quickly charge the filter C and allow for fast settling. This state will last 1us. | pon\_ldo\_txbist=1  pon\_ls\_txbist=1  en\_txbist=1  fast\_enable\_txbist=1 |
| On | The IP is fully active and can be used bist | pon\_ldo\_txbist=1  pon\_ls\_txbist=1  en\_txbist=1  fast\_enable\_txbist=0 |

Table 13: Txbist functional power-states

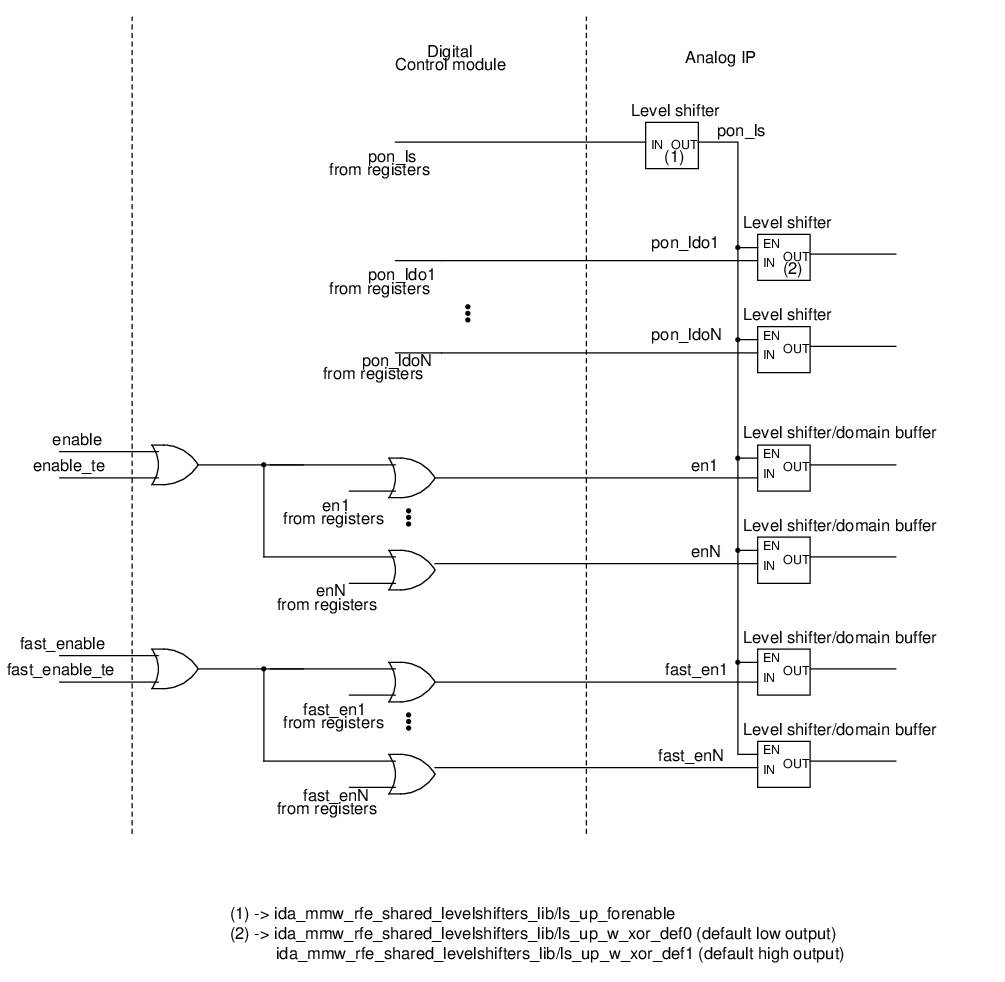


Figure 36: control of the Bist IP

## Interface with external

|  |  |  |  |
| --- | --- | --- | --- |
| pin | type | description | From/to |
| rfin1\_0 | analog | RF input 1 positive | TX |
| rfin1\_180 | analog | RF input 1 negative | TX |
| rfin2\_0 | analog | RF input 2 | TX |
| rfin2\_180 | analog | RF input 1 negative | TX |
| atb1n\_out | analog | Output negative (ATB1) | ATB |
| atb1p\_out | analog | Output positive (ATB1) | ATB |
| atb2n\_out | analog | Output negative (ATB2) | ATB |
| atb2p\_out | analog | Output positive (ATB2) | ATB |
| adctx\_out\_n | analog | Output negative (TX) | ATB |
| adctx\_out\_p | analog | Output positive (TX) | ATB |
| d\_testsw\_en | out | activate the path to settling time comparator | dig |
| D\_txbist\_test\_out\_ls0v9 | out | Output of settling time comparator | dig |
| d\_vga\_ctrl<7:0> | Dig\_in | 7 wires to control of the vga gain | dig |
| d\_txbist\_atb1\_en | Dig\_in | Enable sw to atb1 | dig |
| d\_txbist\_atb2\_en | Dig\_in | Enable sw to atb2 | dig |
| d\_txbist\_atbtx\_en | Dig\_in | Enable sw to tx | dig |
| d\_txbist\_out\_atb1\_en | Dig\_in | Enable sw vgaout to atb1 | dig |
| d\_txbist\_out\_atb2\_en | Dig\_in | Enable sw vgaout to atb2 | dig |
| d\_txbist\_atb1<10:0> | Dig\_in |  | dig |
| d\_txbist\_atb2<10:0> | Dig\_in |  | dig |
| d\_txbist\_mixer\_en  d\_txbist\_vga\_en  d\_txbist\_bias\_en  d\_txbist\_test\_en | Dig\_in | bias  test  vga  mixer\_core | dig  dig  dig  dig |
|  |  |  |  |
|  |  |  |  |
| d\_pon\_ls\_txbist | Dig\_in | enable the level shifters at the interface (1.5V->0.9V). | dig |
| ibias\_txbist\_flat | in | 90uA bg current from Gbias(2% trimmed) | analog |
| ibias\_txbist\_ptat | in | 90uA ptat current from Gbias(2% trimmed) 0.213uA/K(see **[[3]](#footnote-3)**) | analog |
| ibias\_txbist\_bg | in | 20u bg/R | analog |
| d\_xor\_out<1:0> | out | Ls xor out | dig |
| d\_txbist\_spare<10:0> | in | Spare bits | dig |
| txbist\_test\_current\_in | in | Current from tester | analog |
| Supplies | | | |
| vdda\_txbist\_1v8 | supplies | ATB supply |  |
| vdda\_txbist\_1v45 | supplies | LDO supply | GLDO |
| vdd\_txbist\_0v9 | supplies | 0.9V supply for interface |  |
|  |  |  |  |
| vssa\_txbist | supplies | Mixer/vga analog ground |  |
| vssd\_txbist | supplies | Digital ground |  |
|  |  |  |  |

Table 14: interface with external

## Description of the block

TXbist is placed between 2 TX to measure the phase between 2 transmitters. There are 3 TXbist inside the circuit. The phase is sampled thanks to the ADC of the ATB. Care must be taken between the buffer and the ATB ADC (settling time, resistance …)

The block concept is a mixer so the output is :

Vout=A.cos(1).cos( 2)=A.cos( 1- 2) where 1 and 2 are resp the phase of TX1 and TX2. A is the output voltage of the mixer. It depends on input amplitude of TX and the gain of the mixer. A post FFT is done in software to measure the phase of the signal. The SNR must be high enough to measure accurately the phase difference in digital. The VGA amplifies the signal so that the SNR is not affected by the ADC. The output of the buffer is differential with a common mode equal to the ADC input.

### Line up

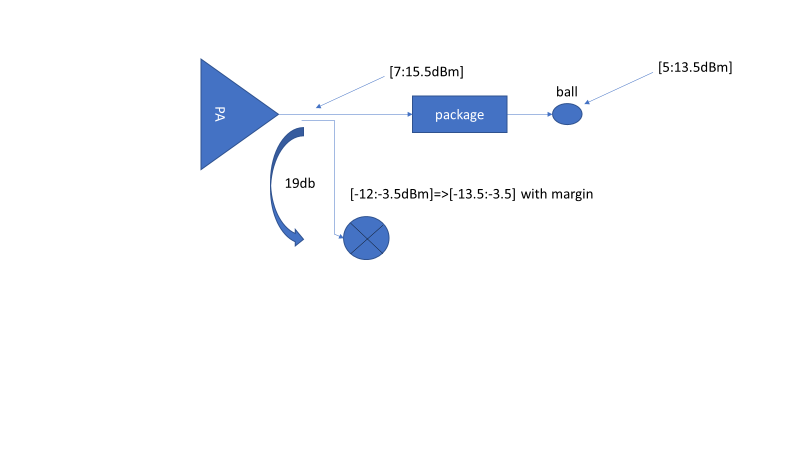


Figure 37: Line up txbist

## Supplies

LDO 0.9V

1.8V for ATB switch

## DFT

### General

Ahead any functional/structural measurements, the LDOs have to be trimmed. The trim strategy is described in the Global bias chapter of the DfT AS.

The SCAN covers the digital parts of BiST IP as per DfX rules.

All buffers, mixers, VGA, PPD detectors and LDOs will embedded accesses to key voltages. They are connected to the DC-ATB bus to be measured with the BiST-ADC. These voltages are defined with the designer to achieve the coverage in the order of magnitude of about 70% with DOTTS. At the time of writing, 04-June-2020, the schematic isn’t mature enough to define precisely these voltages.

The TX output power is measured thanks to a power detector behind a directional coupler. The isolation of the coupler is a contributor of TX output power measurement uncertainty. It cannot be measured. It is taking into account in offsets between the DfT and the UDI RX gain measurement. The repeatability limitation have to be taken into account in the TX output power limit guardbands.

The current consumptions of all subblocks have to be performed in the context of the structural tests. The sum of consumption for the relevant blocks can be performed at the ATE to cover the BiST-IP Doors requirements.

Some signals are sent to the ATB and used for the functional safety [[artf1200730](https://doorsng.nxp.com/rm/resources/MB_0dd8220ee3cf4092a97a85d5d341ccf5?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) ]:

LDO 0.9V

the SNR sums the noise from the RX ADC and the BiST IF DAC. The noise is random over the frequency range. The noise from the RXADC cannot cancel the one from the BiST IF DAC.

There are 8 RX ADC (two per RX channels). It is unrealistic that a defectivity affects the magnitude of the BiST IF DAC and it is compensated by the 8 RX ADC by another defectivity.

The current consumptions of all subblocks have to be performed in the context of the structural tests. The sum of consumption for the relevant blocks can be performed at the ATE to cover the BiST-IP Doors requirements.

Some signals are sent to the aTB and used for the functional safety [[artf1200730](https://doorsng.nxp.com/rm/resources/MB_0dd8220ee3cf4092a97a85d5d341ccf5?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) ]:

LDO 0.9V

### Settling time measurement of the phase rotator

A specific circuitry is composed of a comparator to compare with an external threshold generated by the ATE.

The reference is provided by an external current creating an offset in the comparator. The output of the comparator is accessible through the ATB. The fine value of the threshold is found by the ATE which allows to commute the comparator to a final phase P2. Then the tester programs a phase P1 and then again the Phase P2. The time difference between the final programming P2 and the comparator trig correspond to the settling time.

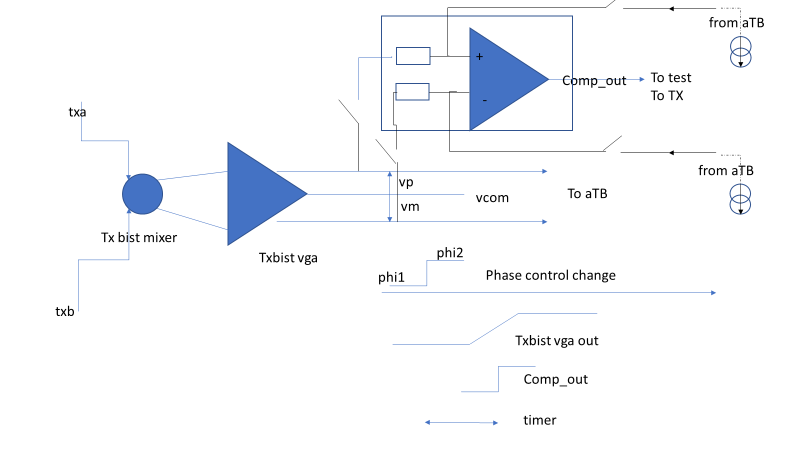
The comp\_out is sent to the TX as digital input that is taking care of connecting it to a GPIO and also a timer integrated in the TX digital.

Figure 38: Additional circuitry for settling measurement on aTE

## Accuracy of the TXBIST function

### Phase reference

The error of phase measurement is defined as in Figure 21. The err is depending on the process variation and is linked to different contributors (mixer, coupler ,lines, ADC, PR INL, PR calibration repeatability) and also to the way it is processed. If we consider the delta phase variation between TXs, The absolute error is not a problem for the application considering that this error is one of the error in the radar system. For example the antennas and mechanics create error that need to be calibrated on the production error. But in production it would be nice to measure the phase difference statistic.

The variation of the error (in time, temperature ) is a problem since it can not be compensated later.

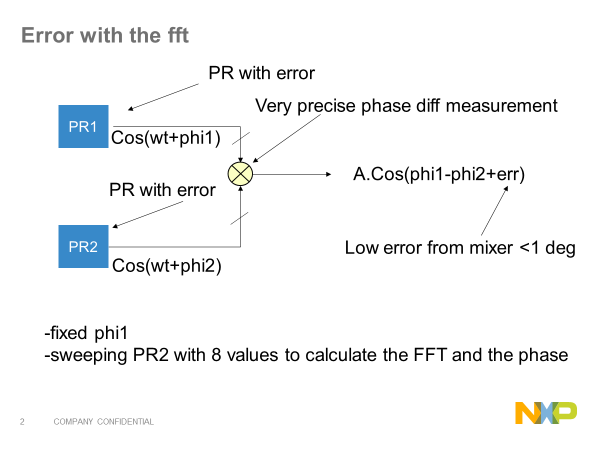


Figure 19 mixer error

### Phase difference variation (safety)

The ph/ph system is based on req 1099005 :

The TX RFBIST shall be able to characterize the relative Phase Difference between the transmitters over the RF frequency band excluding initial detection errors of the TX RF BIST with an accuracy of+/1 deg.

So it is considered that for each IC, we can have an initial error. The system must track the variation of this error so measurement +/-1 deg corresponds to accuracy related to temperature, aging, frequency

Sources of errors :

* Mixer error : corresponds to phase error variation due to aging, frequency, supply, temperature. If we do a PVT or a MC (local/global), for each trial we do a V,T,F change and check the delta error variation between channels. The absolute error has no interest. Notice the final error would be the variation difference between TXBISTs.
* Coupler error : corresponds to the phase error variation due to aging, frequency, supply, temperature. We need a tb with 2 TX, do a mismatch and check V,T,F variation on each run-probably neglectable
* Coupler error due to load (tester) : corresponds to phase error variation due to frequency, supply (test is done at 1 temperature) when the 2 TX are loaded differently (1 TX match, 1 S11 7dB). We checked that the initial error is not changing in this condition due to frequency , supply.
* Phase rotator calibration error: correspond to the phase init step introduced by the calibration from frame to frame
* If the phase difference variation is measured by sweeping the phase on a reference channel and doing the FFT, the variation of the error mismatch between channels vs VT can lead to additional error-neglectable
* Error due to the ADC

### Phase step

The phase step accuracy depends only on the linearity of the phase out vs phase in response. If the response is linear the error of offset are suppressed by the relative measurement. The INL/DNL of the response gives the accuracy.

One major contributor is the reference channel that after calibration brings +/-INL/2

Other contributor is the noise introduced on the TXBIST and the number of points selected to generate the IF and computes the FFT. Error estimation is around 0.5º

### Phase init

The TX RFBIST shall be able to characterize the Phase Difference between the transmitters over the RF frequency band

Sources of errors :

* Mixer error : corresponds to phase error variation due to PVT
* Coupler error : corresponds to the phase error mismatch between 2 transmitters
* Coupler error due to load (tester) : corresponds to phase error variation due to frequency,supply (test is done at 1 temperature) when the 2 TX are loaded differentely (1 TX match, 1 S11 7dB). We checked that the initial error is not changing in this condition due to frequency , supply.
* Error due to the aDC
* Reference Channel error : if measured through fft

## Electrical specifications

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | min | typ | max |  | Linked Doors RS | comment |
| Specification for the RF part | | | | | | |
| Supply provided by LDO | -7% | 0.9 | +7% | V |  | +/-5% full performance, +/-7% full fonctionality |
| Safety supply | -7% | 1.8V | +7% |  |  | +/-5% full performance, +/-7% full fonctionality |
| Input LDO supply | 1.45V-7% | 1.45V | 1.45V+7% | V |  | +/-5% full performance, +/-7% full fonctionality |
| input power | -13.5 |  | -1.5 | dBm |  | To cover the high range of PA |
| Input difference level at mixer |  |  | 1 | dB |  | In the case of unbalanced TX |
| Output level at vga output | 0.2Vpk |  | 1.2Vpk |  |  | Adc differential range. Min signal for not having the adc limiting |
| Output common mode voltage | 0.38 |  | 0.6 |  |  | Adc common mode |
| Impedance to drive between TXbist and ATB |  | tbf |  |  |  | Line and impedance to drive |
| Vga gain control | 0 |  | 25 | dB |  | Output mixer can be down to 10mvpk single |
| Gain step |  | 5 |  | dB |  |  |
|  |  |  |  |  |  |  |
| TXbist phase difference variation accuracy with V,T,F at specific Pout | -1 |  | 1 | deg |  | For phase difference variation  [artf1099003](https://doorsng.nxp.com/rm/resources/_6f3c4d9a8c244b879137c21948390f78?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| TXbist phase difference accuracy with V,T,F | Tbf | 1.6 | tbf | deg |  | For phase measurement |
| INL/DNL | -0.5 |  | +0.5 | deg |  |  |
| TX phase range | -180 |  | 180 | deg |  | [artf1099005](https://doorsng.nxp.com/rm/resources/_66f75e68812348f092935fc083c984f1?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Isolation between 2 inputs in on/off mode | 10tbc |  |  | dB |  |  |
| Isolation between 2 TXs in on/off mode | 50 |  |  | dB |  |  |
| SNR at VGA output | 40 |  |  | dB |  | On 10K-10MHz BW |
| TXbist settling time |  |  | 1.25 | us |  | For fast measurement |
| TXbist settling time with filter bypass |  |  | 50 | ns |  |  |
| Power consumption txbist(on 1.45V) |  |  | 10 | mA |  | [artf120475](https://doorsng.nxp.com/rm/resources/MB_6bea3e4b236d411abd25e7e75dbf4bf8?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Powerdown current txbist(on 1.8V or 1.45V) |  |  | 100 | uA |  | [artf1098963](https://doorsng.nxp.com/rm/resources/_2537cda588e64b9dad25dc7c15980698?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Startup time/powerdown |  |  | 1 | us |  | From poweron to signal out  [artf1204723](https://doorsng.nxp.com/rm/resources/_a1605403c25f48f0b3de45f1dfeb31d4?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
| Silicon area |  |  | tbf |  |  |  |

Table 15: TXBist specification

## Design Decisions (to be logged in DOORS AS)

|  |
| --- |
| TXBIST |
| A system is placed between each transmitters to measure the phase difference |
| A RF mixer is converting the RF difference signal into a DC information (cos(phase)) |
| A VGA is used to amplify the signal when the phase measurement is done for a low RF power |
| The VGA is able to drive the ATB ADC in less than 1us to be able to measure each phases quickly |
| the TX digital postprocessed the analog data converted by the aTB ADC |
| The phase difference is based on the FFT of the difference of the channel under test with the reference channel. The reference channel is swept in phase to get 8 (or 16) phase points. |
| The control and the measurement of the phase (through FFT) is managed by the ARM7. |
| The number of phase differences is controlled by the software |
| Phase difference and also phase steps can be measured through this method |
| The initial phase difference is captured in production and must be taken into memory. Any shift or unacceptable change must create an error by the safety software |

# TXBIST Digital

## Block diagram

TXDIGBIST module is merged within TXDIG module and is sharing with TXDIG SPI2AHB, register map, CRC, OCCII interface

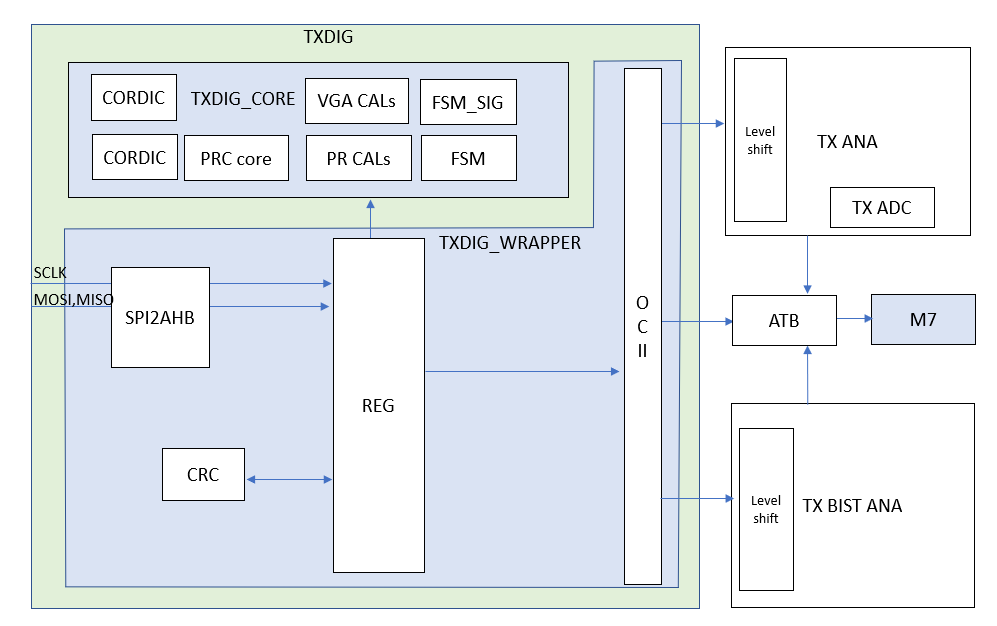


Figure 40: TXDIGBIST merged with TXDIG

## General Functionality and Operational mode

TXBIST is the companion of TX. TXDIGBIST contains SPI registers which control VGA gain(vga\_ctrl), lowpass filter mode by disabling the filter (LP\_dis) of the TXBIST RF module.

TXDIGBIST also controls the enable of the TXBIST level shifter (Pon\_ls\_txbist) , turns on the LLDOs of the TXBIST (Pon\_ldo\_txbist), enable the TXBIST IP(enable\_txbist) , speed up TXBIST enable (fast\_enable\_txbist) and bypass LDO (ldo\_bypass)

Digital content is mostly done in software. ARM7 is controlling the TXDIG phase which is passed through the TXDIG CORDIC and thermometer encoder . 256 thermometric bit are brought to the DAC which controls the rotation of the TX phase through the phase rotator. The TXs PAs outputs are combined in the TXBIST and provide and output to the ATB/ADC. ARM7 is reading back ATB ADC data.

Figure 20: AMR7 Phase measurement loop

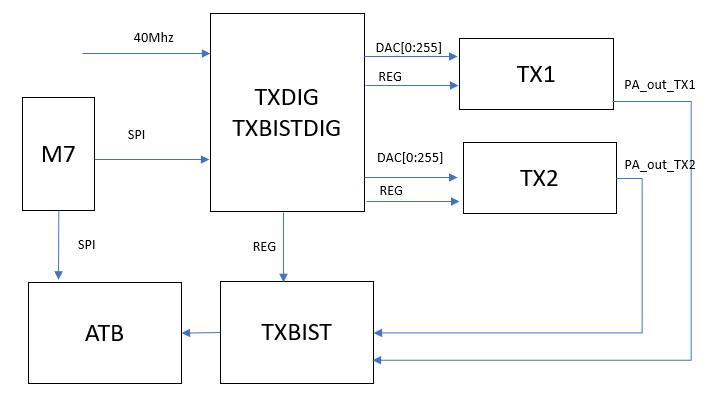


Figure 41: Phase measurement loop with ARM7

## Interface with external

* To safety monitor
  + TXDIGBIST does not interface directly with ISM.
  + Safety mechanism decision is implemented in AMR7
* Via SPI
  + TXDIGBIST SPI register are described 6.3

## Electrical specifications

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| spec | min | typ | max |  | Linked Doors RS | comment |  |
| Max time for TX safety |  |  | 4ms-Tcal | ms | yes | Should be in the total safety budget | [artf1098986](https://doorsng.nxp.com/rm/resources/_1158faa31334446ab92e0b2f1a5baf43?oslc_config.context=https%3A%2F%2Fdoorsng.nxp.com%2Fgc%2Fconfiguration%2F136) |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |

Table 16: Electical specifications TXBIST

# Post processing with ARM and software (calibration and safety)

## General processing

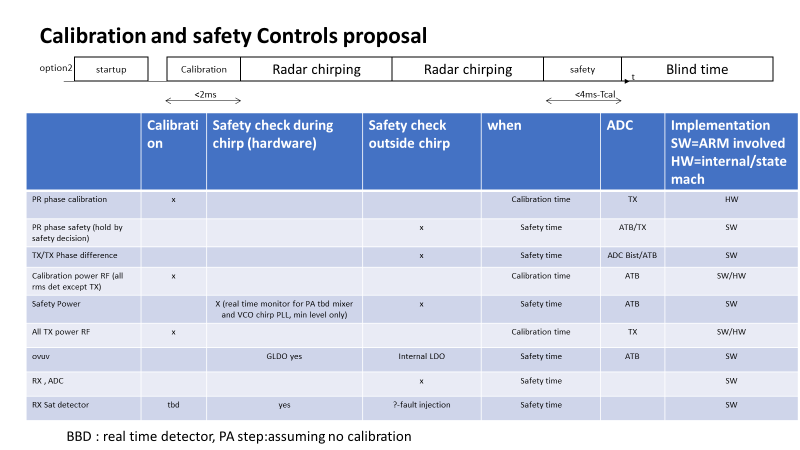


Figure 42: chirp vs Bist (calibration and safety)

### Calibration

To be updated

In the RXBIST several calibration are done by software. Calibration is proposed to be run at each chirp frames. Calibration must be done in this order :

-first LO

-then SSB

#### LO doubler Power calibration

LO feeds LO doubler with a power of -12dBm. In not enough this power can be boosted to -10dBm. Calibration of the output of the LO doubler take this into account as shown in the figure below.

This calibration uses binary search to find the closest power to the targeted one. However we need after each binary search to check that the chosen code is within the limits of calibration accuracy (here power steps of 0.5dBm max).

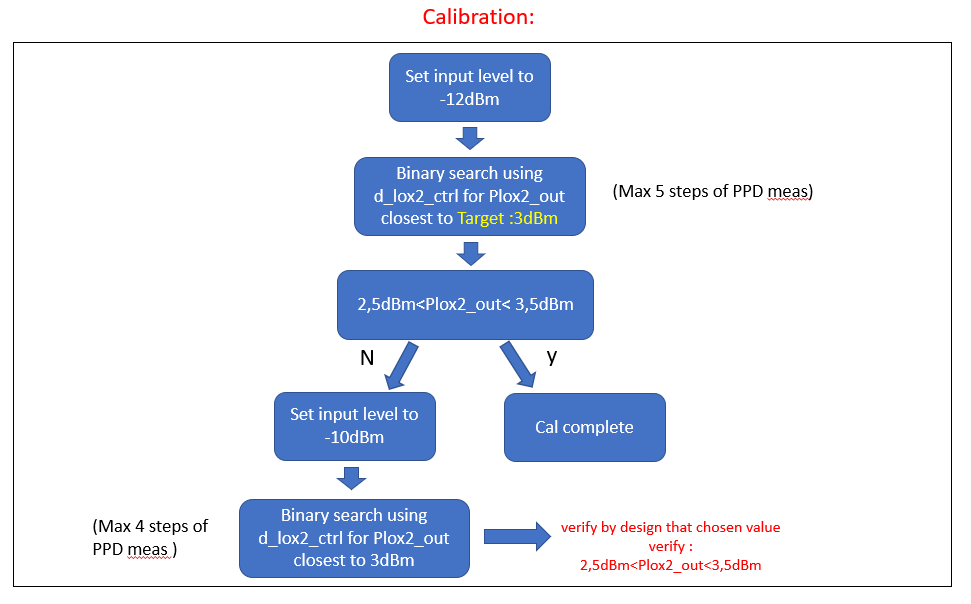


Figure 43: LO doubler power Calibration process

The output Power is measured by the PPD. In the final algorithm the binary search will be done on PPD Vout values. The target (3dBm) and the limits (+/-0.5dBm) will be transformed to voltage values at the PPD. PPD accuracy will then be added to the result.

(to be updated with real ppd accuracy)

#### SSB output Power calibration

Output Power of SSB must be calibrated to have a measurable voltage at PPD level in the Rx (>140mVpkdiff or >-15dBm). In a similar way we can calibrate using the PPD at the output of SSB while targeting an equivalent output power of 4dBm (see ch 4.4.1).

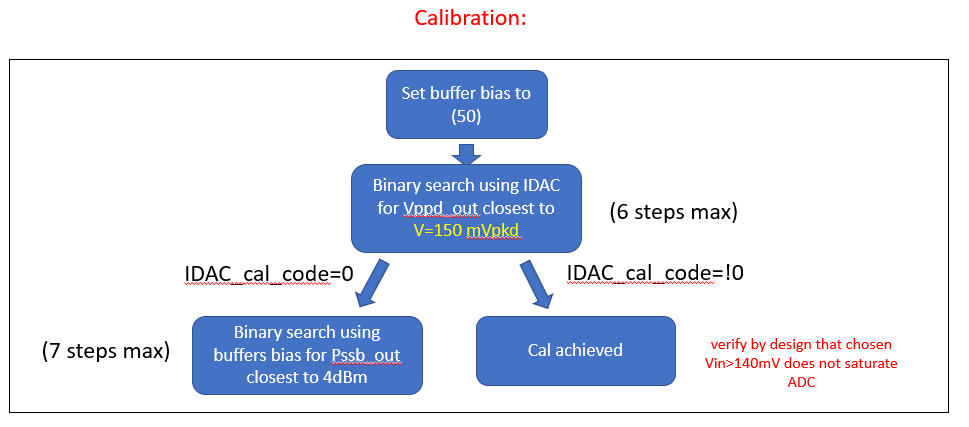
 In this calibration, there is two controls for the power: PR DAC current IDAC and Buffers 1, 2 and 3 biases. This late ones are controlled all together with SSB\_gain\_buffer control.

Figure 21: SSB output power calibration

Due to design consideration, Iref DAC must be used first to set the targeted power. If the minimum value of Iref\_DAC cannot achieve the target, SSB\_gain\_buffer is then used. This order is necessary to desaturate the buffers before controlling the biases.

Figure below shows the calibration algorithm using Rx ppd with a targeted calibration value of 140mVpkdiff.

#### Power detector calibration

Not defined yet if needed

#### Sat detector Calibration

This saturation detector calibration is proposed to be run at startup only

* Bist power calibration:

Sat detector calibration start by calibrating BB Bist power for all power steps used in this calibration. If this calibration is already done. This step is bypassed.

- rx switch config 2: calibration to ADC

- Set attenuator to 5dB or 10 dB attenuation.

For k=0:kmax {

- Set bist voltage to VBist\_k=Vmin+k\*Vstep,.

- Read ADC output voltage and store the result.

}

* Gain compression 1dB measurement:

Pout\_1dB of VGA1 is then measured through a binary search for all PBist\_N powers:

- VGA1 at max gain

- Rx switch config 4-a (See table XX), switch on attenuator Sw5 (5 to 10 dB).

For k=0:kmax {

- Set bist voltage at

- Read ADC output voltage and store the result. (n for receiver n=1,2,3,4)

}

* determine k0 such as =1,12

N.B: binary search cannot be done here since binary search need monotonic measurement. the result of last step will be close to the threshold and can cross it in a non-monotonic way.

* Sat detector level calibration:
* Set Sat detector level to it’s min
* Set Pbist=PBist\_Nsat-Pguardband
* Increase sat detector level until saturation flag is on
* Set BB power to PSatDet=Pout\_1dB-P\_guardband
* Increase saturation detector level until clipping

Need to define Nmax, Vstep, Sat\_step, Vguardband

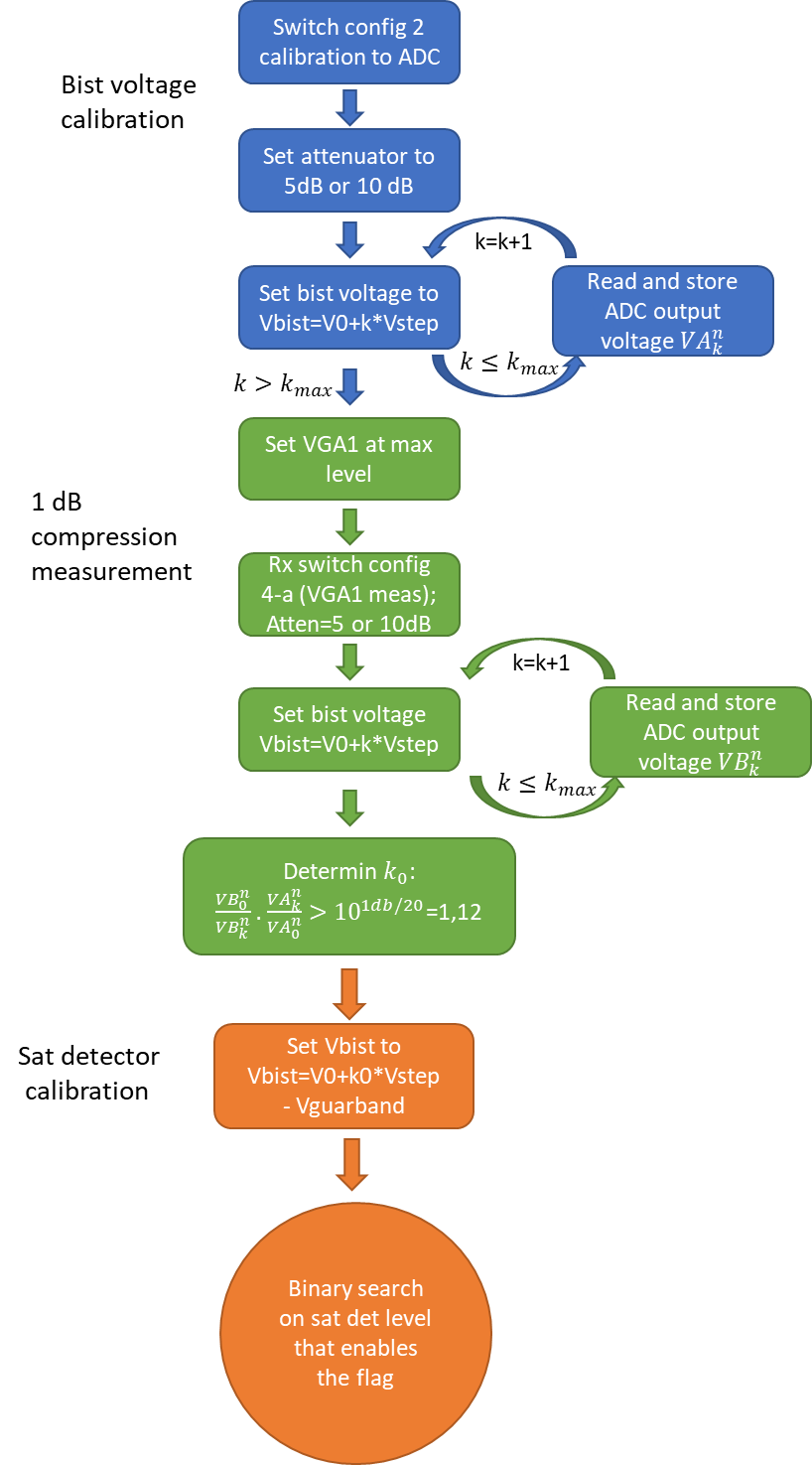


Figure 44 : Sat detector calibration state machine

## RX safety

To be updated

### Description of tests planned for safety

In the following, index n in is used for the nth receiver n=1,2,3,4

For calculus saving, all measurement are done in linear domain

#### RF gain/phase measurement

* Minimum Gain measurement using ppd (as reference)

- set all RX on , use min gain setting for VGA

- set SSB modulator max power and program frequency IF with respect of 5.3.1

- measure the voltage at 4 power detectors at RX input

- measure the 4 FFT bin at IF

- calculate minimum gain : n=1,2,3,4 for 4 receivers

* Gain/phase measurement

- set the SSB power to

( is the adequate power to not saturate the vga at gain and such as the SNR at ADC in is >30dB at for good accuracy measurement)

- measure the 4 FFT bin IF ), n=1,2,3,4

- set IF gain to Gi

- measure the 4 FFT bin IF n=1,2,3,4

- calculate gain I : ; n=1,2,3,4

- calculate phase i:

#### Measure AGC steps/gains (using IFBist)

In the following, is the adequate bist output power that not saturate the VGA/ADC at gain and such as the SNR at ADC in is >30dB at for good accuracy measurement

Set the SSB IFBIST power to Pi

- measure the 4 FFT bin IF ), n=1,2,3,4

- set IF gain to Gi

- measure the 4 FFT bin IF n=1,2,3,4

- calculate gain step i : ; n=1,2,3,4

#### Measure the NF

the noise figure is measured at a given gain

- Rx bist is off

- set the AGC to gain

- capture signal with nfft samples

- calculate fft of the captured samples for each Rx

- Measure the noise in the bandwidth (quadratic mean of all fft bins in the bandwidth)

-Calculate noise figure where is reference noise

#### HPF

-set nominal gain

- set ADC to 10Ms/s to minimize the number of samples of the fft

- select square mode generation for RFbist with a low frequency

must be in the bin of the sampled signal at 10Ms/s:

where is the number of samples take for the fft.

Given to 8.2.3, must be at least 256 point, and the lowest possible to achieve 5% accuracy in frequency measurement.

Good value: ; ; 🡪 (p=1) or (p=3)

- do ftt on samples for each Rx

- measure the level of the bin frequency at 5\* for each Rx n

- Do binary search on the bins for the nearest levels to . The binary search range can be reduced to bins between ; where is the theoretical frequency we are looking to estimate.

- The frequency bin of the nearest level above is a good estimation for

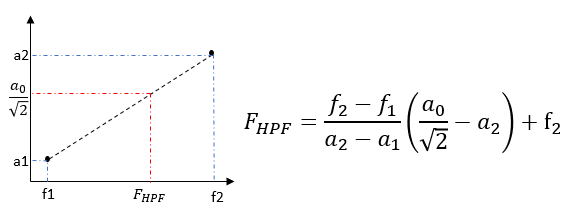
- For more accuracy, linear interpolation between the two nearest values can be done to estimate as shown below:

Figure 45: estimation of HPF with linear interpolation

Table below gives simulation results for different configurations:

Table 17: HPF frequency accuracy

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | fft size: | 128 | 256 | 512 |
| Error [%] | Nearest point | 30 | 8,8 | 5,6 |
|  | Linear interpolation | 15,5 | 4,6 | 2,7 |

#### RX linearity

-Set BBBist input vga switch

-select 2 tones modes for BBBist IF1,IF2 and levels

-measure the bins of 2IF1-IF2 and 2IF2-IF1

#### ADC purity

-Set BBBist input vga switch

-select 1 tone with level and frequency

-check the spectrum

#### Sat detector

* Sat VGA1 at max gain
* Set BBBIst voltage to (see chap 8.1.1.3)
* Check sat detector flag is on

### ARM 7 FFT processing

Processing of measurement of is done in the ARM7 processor run at 160MHz clock.

ADC samples are stored in 2\*16kb DMA memory. Each sample is 16 bites=2bytes. Memory can handle up to 8000 samples coming from 4 Rx channels with simultaneous acquisition.

Once samples stored, ARM7 allow some fast postprocessing. Table below summarize fft duration time for 1 channel different configurations(valid for 1 channel).:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Single bin FFT | | |  | Full size real FFT | |  |
| Real SBDFT size | ARM instruction cycles | Time duration [us] |  | FFT size | ARM instruction cycles | Time duration [us] |
| 1024 | 2068 | 13 |  | 1024 | 40108 | 251 |
| 512 | 1044 | 7 |  | 512 | 15946 | 100 |
| 256 | 532 | 3 |  | 256 | 7660 | 48 |
| 128 | 276 | 2 |  | 128 | 3098 | 19 |
| 64 | 148 | 1 |  | 64 | 1719 | 11 |
| 32 | 84 | 1 |  | 32 | 676 | 4 |
| 16 | 52 | 0 |  | 16 | 185 | 1 |
| 8 | 36 | 0 |  | 8 | 118 | 1 |

Table 18: FFT time

### FFT size and accuracy for RX measurement

Table below gives some measurement processing parameters and accuracy results. Acquisition time corresponds to sampling point\*Number of points

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | SBDFT size | FFT Time [us] | Acquisition Time [us] | Comment |
| RF gain from Lna to ADC | Single Bin 256 Samples | 3 | 3,2 | precision +/-0,1dB |
| NF | Full SBDFT 512 | 100 | 6,4 | precision +/-0,5 dB |
| Rx Phase difference | Single Bin 256 Samples | 3 | 3,2 |  |
| AGC gain | 7\*Single Bin 256 Samples | 31 | 29,4 | precision +/-0,1dB |
| RX linearity /IMD | 3 bins \* 256 samples | 9 | 3,2 | precision +/-0,1dB |
| ADC purity | Full SBDFT 256 | 48 | 103 | 10MHz Sampling |
| hpf | Full SBDFT 256 | 48 | 103 | 10MHz Sampling; 5% precision |
| Sat detector calibration | 10\*Single Bin 256 Samples | 30 | 42 |  |

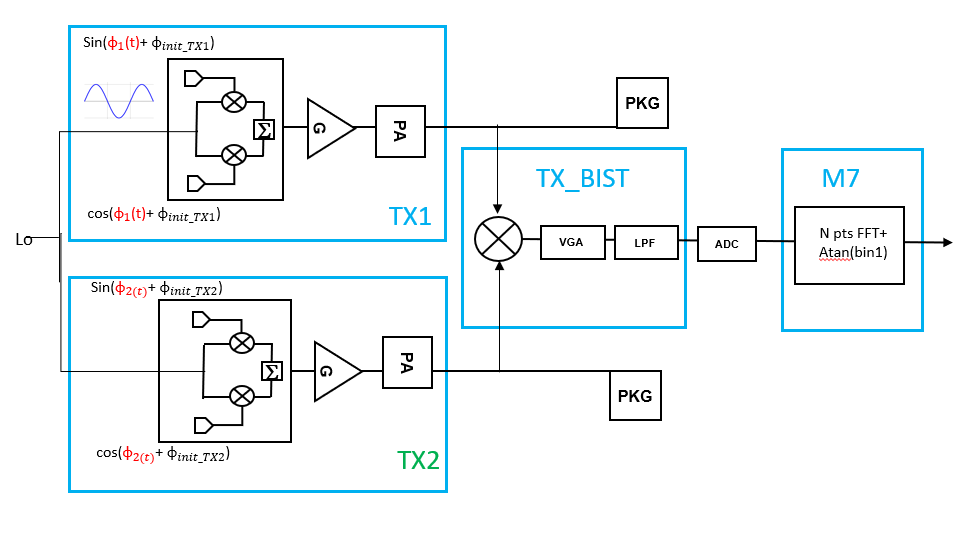
Table 19: FFT size

### Total time for RX safety

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **Duration using different register access methods [us]** | | | **number of registers access** | **number of elements** | **numb of ADC(optimization)** |
| **Bist** |  | **AHB access** | **160 MHz SPI** | **40 MHz SPI** |  |  |  |
| **general configuration** |  |  |  |  | **?** |  |  |
| RX gain from LNA to aDC |  | 16 | 18 | 23 | **5** |  |  |
| NF |  | 407 | 409 | 414 | **5** |  |  |
| Rx Phase difference |  | 16 | 18 | 23 | **5** |  |  |
| AGC gain |  | 160 | 168 | 190 | **21** |  |  |
| RX linearity/IMD |  | 40 | 42 | 47 | **5** |  |  |
| ADC purity |  | 206 | 208 | 213 | **5** |  |  |
| hpf |  | 296 | 298 | 303 | **5** |  |  |
| sat detector |  | 17 | 19 | 24 | **5** |  |  |
| Total |  | 1160 | 1179 | 1238 |  |  |  |
| TX phase2phase difference |  | 109 | 158 | 314 |  |  |  |
| TX phase step measurement |  | 291 | 418 | 826 |  |  |  |
| Total |  | 400 | 576 | 1140 |  |  |  |
| PPD monitoring through ATB ADC |  | 35 | 56 | 125 | 4 | 33 | 2 |
| Local LDO: OV/UV detection (through ATB ADC) |  | 21 | 34 | 76 | 4 | 20 | 2 |
| Total |  | 56 | 90 | 201 |  |  |  |
| Core self test |  |  |  |  |  |  |  |
| Peripheral tests |  |  |  |  |  |  |  |
| PLL frequency/ lock/unlock? |  | 0 | 0 | 0 |  |  |  |
|  | **Σ** | **1615** | **1845** | **2579** | **[us]** |  |  |
|  |  |  |  |  |  |  |  |

## TX Safety

### Phase measurement principle



The chapter describes the way a phase is measured.

Figure 44: TX Safety mechanism

The 2 TX outputs are combined within TXBIST module

In TXBIST, the baseband signal is amplified through a VGA , filtered by a lowpass filter to limit the out of band noise and passed through an ADC. The digital outputs of the ADC is stored with a ARM7 which post process the data through FFT and Atan trigonometric function to compute a phase.

N phases are applied on first TX. Those N phase are describing a 1 period signal (IF) with a phase step of 360/N º .

On second TX is applied a fix phase Φ2

The down converted signal is a N points signal with phase Φ2 information: cos(IF+Φ2)

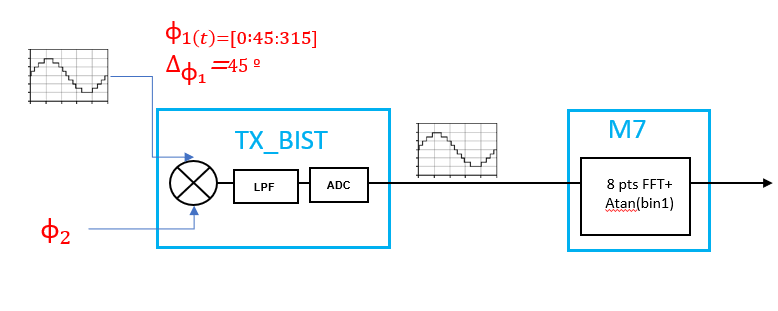


Figure 45:TX BIST example with N=8

A N points FFT is performed on the down-converted signal. Output of the FFT is a complex signal of N points which represents N frequential bin.

Bin1 contains the information of the fundamental of the IF signal . The phase is the output of the Atan of bin1.

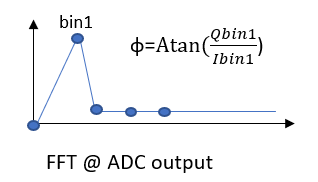


Figure 46: Phase computation from FFT

### TX to TX delta phase variation.

#### Block diagram

The “TX to TX delta phase variation ” safety mechanism measures the variation of the phase init between 2 TX. If the delta phase variation is higher than a defined threshold, a flag is asserted.

The design under test are the 2 TXs .

The measurement mechanism is composed by the TX BIST module, the ATB ADC and post processing in the ARM7

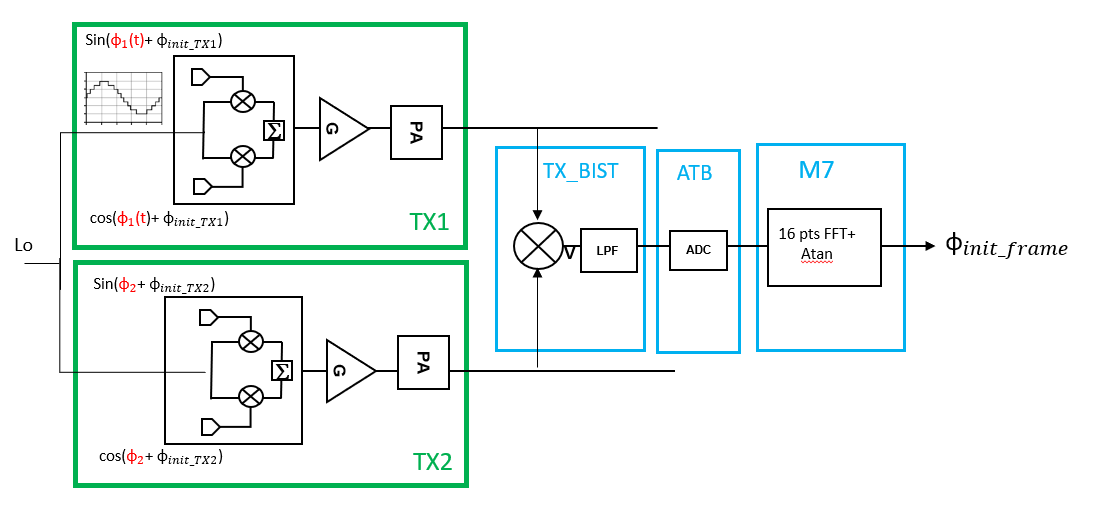


Figure 47: TX 2 TX delta phase variation block diagram

#### TX to TX delta phase variation principle

In the context of safety 1 phase shall be measured using the process described chapter 8.3.1 .

The first TX is used to generate the IF. In the context of safety, the IF is described using 16 phase = . The FFT shall be done using the same number of points.

The fix phase of the second TX shall be selected in the range [0:360]º

phase init Φinit is computed at the end of each frame.

The reference phase is a phase\_init measurent stored in OTP or register.

The delta phase is defined as the difference between the phase init (Φinit) computed at the end of each radar frame and a reference phase.

The delta phase variation is defined as the variation of delta phase over Radar cycle.

#### Error on TX to TX delta phase variation

The safety mechanism is adding uncertainty on phase measurement .

The maximum error estimation is 1.8º

#### TX to TX delta phase variation algorithm

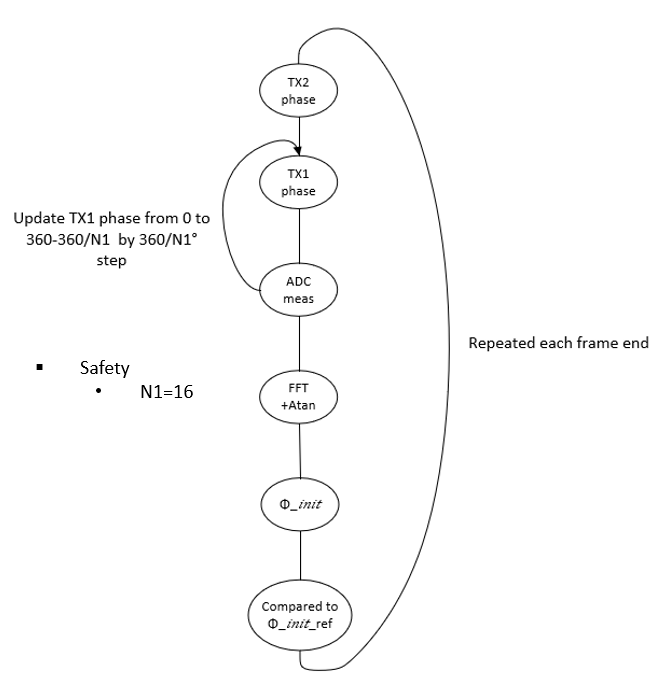


Figure 48:TX 2 TX delta phase variation algorithm

#### TX to TX delta phase variation sequence

TX to TX delta phase variation is done by creating successive pairs of the 4 TX.

The mechanism is a 3 steps approach

Step1:

IF is generating on TX1 , Fixed frequency on TX2

Step2:

IF is generating on TX2 , Fixed frequency on TX3

Step3:

IF is generating on TX3 , Fixed frequency on TX4

One only ATB ADC I used during the safety check.

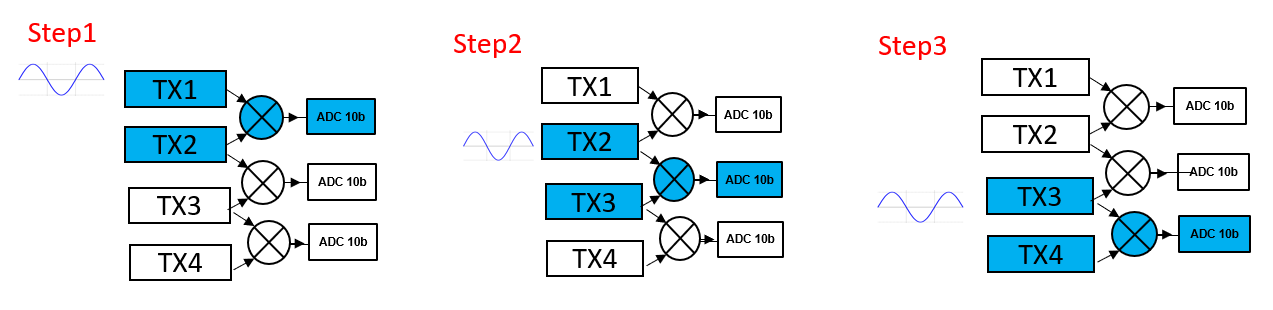


Figure 49: Tx2 TX delta phase variation sequence

#### TX to TX delta phase variation safety time

The estimation time using a 160MhzSPI access is 158us using a 16points FFT.

### TX Phase step measurement

#### Block diagram

The “TX phase step” safety mechanism measures the phase step between 2 successive phase code applied on a TX .accuracy on the measurement is 1.6º . If the phase step is higher than a defined threshold, a flag I asserted.

The design under test is 1 TX .

The measurement mechanism is composed by 1 TX module(different from the DUT) , the TX BIST module, the ATB ADC and post processing in the ARM7

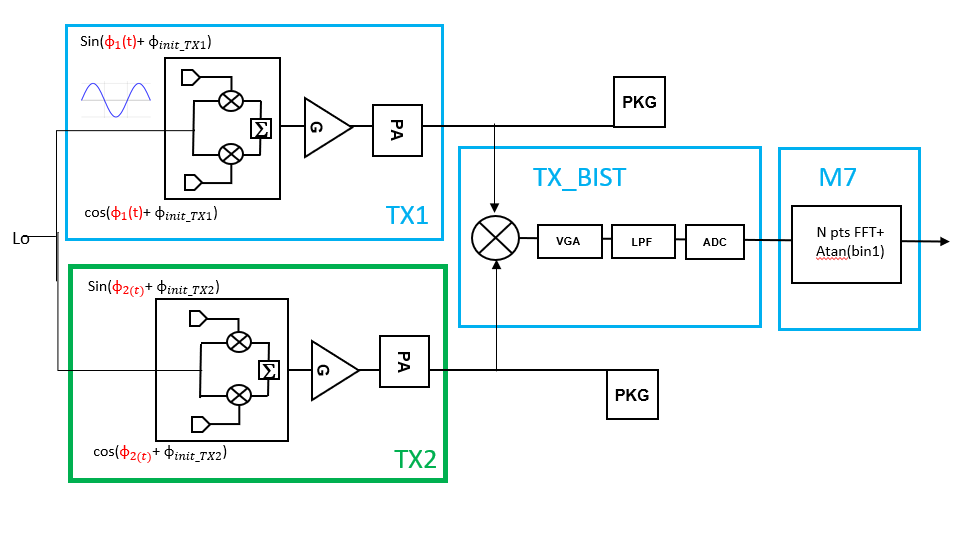


Figure 50: Phase step block diagram

#### Tx phase step principle

In the context of safety 8 phases shall be measured using the process described chapter 8.3.1 .

Those 8 phases could be by example = .

The first TX is used to generate a “pseudo IF” signal. In the context of safety the IF is described using 8 phase = . The successive difference of the input phase of the first TX is *=*45 º. The FFT shall be done using the same number of points than the one used to generate the IF.

for each of the input phase an output phase is computed through the FFT (single bin DFT+atan). The successive difference of those output phase - are compared to the successive difference of the input phase . If the difference is higher than a predefined threshold a flag is asserted preventing on a failure in the rotation of the phase of the TX.

#### Error on phase measurement

The safety mechanism is adding uncertainty on phase measurement .

The maximum error estimation is 1.6º

#### TX phase step algorithm

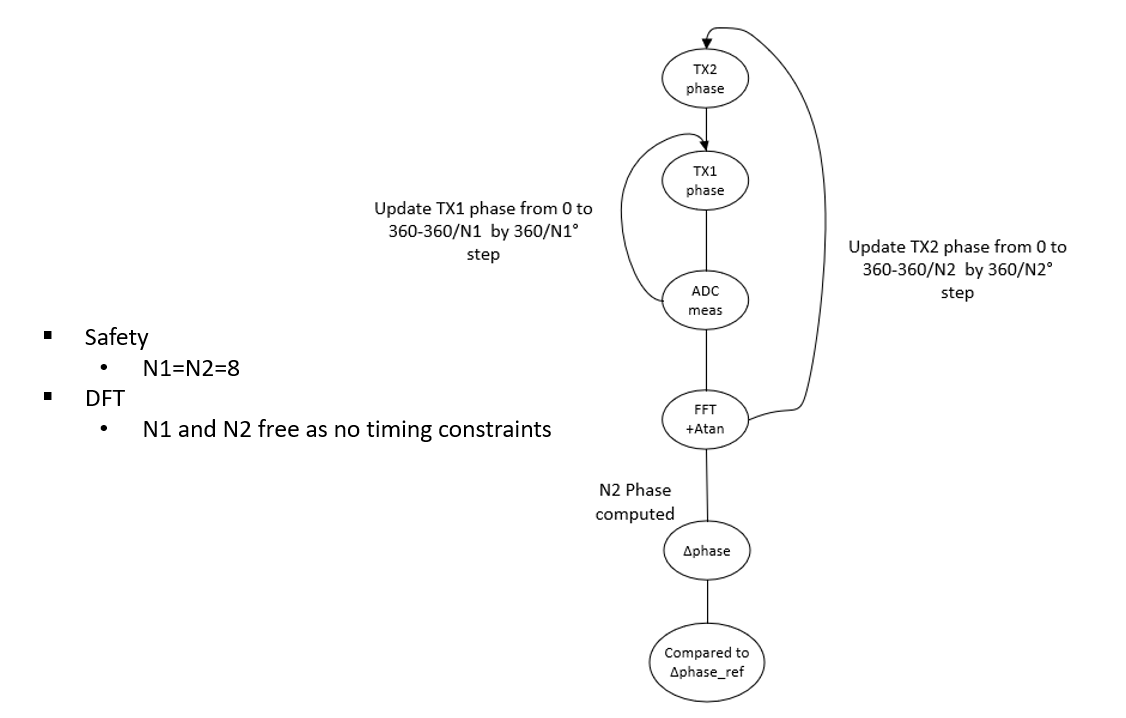


Figure 51: Tx phase step algorithm

#### TX phase step sequence

Phase step is done by combining TX by pair.

TX1 is combined with TX2

TX3 is combined with TX4

The mechanism is a 2 step approach

Step1:

IF is generating on TX1 , Fixed frequency on TX2

IF is generating on TX3 , Fixed frequency on TX4

Step2:

IF is generating on TX2 , Fixed frequency on TX1

IF is generating on TX4 , Fixed frequency on TX3

Both pairs are assigned to 1 ATB ADC to minimize the safety time

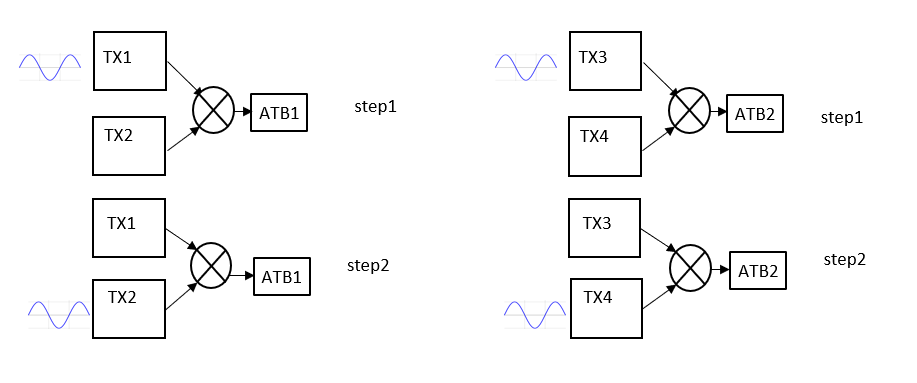


Figure 52: Tx phase step sequence

#### TX phase step safety time

The estimation time using a 160MhzSPI access is 418us using a 8points FFT.(considering to ADC/ATB are used in parallel)

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1. Initial Spec can be found in <https://www.collabnet.nxp.com/sf/docman/do/viewDocument/projects.smarttrx/docman.root.es0.011_ic_architecture_design_and_i.ip_design.ams_ips.global_bias/doc421749?selectedTab=review> [↑](#footnote-ref-1)
2. More precisely, the ratio of the IF amplitude and the number of unit-cells. [↑](#footnote-ref-2)
3. Initial Spec can be found in <https://www.collabnet.nxp.com/sf/docman/do/viewDocument/projects.smarttrx/docman.root.es0.011_ic_architecture_design_and_i.ip_design.ams_ips.global_bias/doc421749?selectedTab=review> [↑](#footnote-ref-3)